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Single-Port 5T SRAM Cell for Signal Processing: Design and Optimization

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***Abstract*—**This has made SRAM more than a memory for logic LSIs, as it runs at very high speeds and draws almost no power in standby mode. The Above is a new 5T single-port SRAM cell with integrated helper circuitry.ŕ,In order to improve on the writing efficiency and avoid unnecessary energy wasting, the novelty of this device is founded on considering two-phase scanning and provides an efficient solution toward the writing "1" problem.The parasitic leakage current in standby mode is meant to be constantly kept low in the standby starting circuit design. The performance and advantages of the new method are confirmed by the results from simulation**s.**

Keywords—Signal-processing systems, Memory stability, leakage power, Elevated-density embedded systems, noise margin, Scalability, efficiency.

I. INTRODUCTION

A static random access memory (SRAM) cell is the basic building block of the SRAM array, which is capable of writing, non-destructive reading, and data storage. The only real problem with SRAM is the transistor overhead. It has thus become desirable to recommend an SRAM cell to work with a lesser number of transistors. The mode of operation of SRAM cells is: write, read, and standby. The information in the SRAM cell is stored upon writing, and information from the SRAM cell is read. Writing a logic "1" while already holding a logic "0" can present difficulties when a single-ended bit line is used in SRAM cell write operations. The data stored in the SRAM cell is initially stabilized when the power supply voltage, VDD, is introduced to the cell's voltage lines within the control circuits. To facilitate reading from the SRAM cells, this power supply voltage is pre-charged to the bit line (BL) by activating the access transistor through a signal applied to the word line.

Conversely, applying ground voltage via the word line disables the access transistor, preventing any interference from the SRAM cell during reading operations. The coupling of a higher potential to the bit line against a lower potential during read operations may lead to the destruction of stored data if the line is decoupled from the bit line, BL.

Additionally, during the standby mode, it can produce unwanted standby power losses through dangling currents. This leads to these currents accounting for a considerable amount of total power consumption as CMOS technology advances into the area of 90-nm and below [9]. Overall, there are three categories of leakage in a MOS transistor: sub-threshold leakage, gate leakage, and reverse bias junction leakage [5]. As the dimensions of the MOS transistors begin to shrink, any from the aforementioned sources will eventually rise, contributing to increases in total power consumption because of the rise in leakage current. Strong SRAM cell architecture with little leakage is therefore highly critical. The stored data gets corrupted because the procedure is disconnected from the bit line BL. The leakage current can also cause unwanted power dissipation due to standby mode. When it comes to scaling down to 90 nm and below, CMOS technology will face increasing contributions to power loss from leakage.

More than half of the total power dissipation would be contributed from leakage currents [9]. Sub-threshold leakage, gate leakage, and reverse bias junction leakage are typically the three main forms of leakage in a MOS transistor [5]. The on-state of smaller MOS transistors results in lesser cut-off and sub-threshold leakage whereas Reverse Bias Junction and Gate leakage increase. The overall effect of the scaling of designed for moderate-sized SRAMs must be to maximize the trade-off between performance and process.

The structure of the other parts will be as follows. Section II gives a brief description of the 5T SRAM cell standard construction. The 5T SRAM cell is discussed and analyzed in section III, which presents the 5T SRAM cell integrated assist circuits. Simulation results are used in Section IV to illustrate the merits and effectiveness of the proposed approach. The achievements of this paper have been summarized in Section V.

II CONVENTIONAL FIVE-TRANSISTOR (5T) SRAM CELL

Each typical single-port five-transistor (5T) SRAM cell consists of two INV1 cross-coupled inverters [10], which are schematically illustrated in Figure 1. INV2 and an access transistor, MA1. The access transistor MA1 is connected to the bit line BL and the word line WL. The word line WL is activated to either write data A into node A by driving VBL or to read data A into BL by driving the voltage at node A. Because

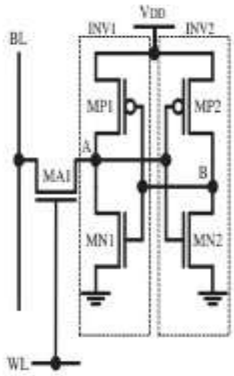

Figure 1. Circuit diagram of the conventional single-port 5T SRAM cell.

MA1 has lower conductance than MN1, it is usually harder to write a "1" if there is already a "0." The access transistor MA1 must be highly conductive in order to prevent a write failure. Specifying the correct form of desired data to be put into the cell. When read and standby activities are in operation, the access transistor's conductivity has to be lowered in order to achieve a favorable stabilization. State conflict between two specifications of the size of the cell transistors. An approach is thus needed such that it enhances the write-ability of the cell while ensuring a high-level of stability during the read operation.

III. PROPOSED5T SRAMCELL CONFIGURATION

A. Description of the Proposed 5T SRAM Cell

The proposed 5T Static Random Access Memory (SRAM) cell and its additional circuitry are depicted in Figure 2. This configuration comprises several essential components: a read/write (R/W) voltage control circuit, a standby start-up circuit, a high voltage level control circuit, a word line voltage conversion circuit, the 5T memory cell itself, and a pre-charging circuit.

This high voltage level supply drive consists of two PMOS transistors, P61 and P62. The two transistors function to utilize VDDH, which is an enhanced power supply voltage. It is important to note that if the threshold voltage (Vth) of the PMOS type transistor is larger than the normal power supply value, VDD, it will definitely influence the much larger power supply voltage VDDH. Moreover, the issue of writing "1" can be efficiently addressed without compromising the reading speed by integrating the R/W voltage control circuit with the high voltage level control circuit.

Define acronyms immediately upon their first instance within the text, even after they have been defined in the abstract. IEEE, SI, MKS, CGS, sc, dc, and rms are not required to be specified in the acronym. It is generally recommended to avoid using abbreviations in the title or headings unless absolutely necessary.

B. The Transients Associated with a Write '1' Operation

To ensure that writing is done successfully, it is essential to keep VA or VB below the inverter trip-voltage. As soon as a "1" is to be written, the voltage of the signal at VBL has been elevated and VWLC kept low. In case a "1" has already been stored, VWLC is first raised to high before writing "1." Transistor M13 gets activated when VWLC crosses the threshold voltage of the transistor VTM13. Since P11 is still on and VBL being high, voltage VA remains VDD until the termination of the writing operation. For writing "0", WLC is low and VBL is high. Once a "1" is detected, the VWLC goes up first for logic on the write "1" action.

When the VWLC crosses the VTM13 threshold voltage, M13 is activated. M11 induces a "1" at VBL, pulling VA all the way up to VDD until the write operation is completed. Next, the charge source moves to storing "0" for VA. This is where VA is sent high by VWLC. Transistor M13 becomes active once VWLC crosses threshold voltage VTM13. Thus, voltage division that includes driver transistors and access transistors will ultimately bring the voltage VA up. The charge shifts when data flip occurs.

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This positive feedback causes a change in the state of the data bit when the voltage is crossed over a specific threshold. Thus, the write "1" problem in the conventional 5T SRAM cell can be solved once the write "1" operation is finished. It can be seen that, when writing a logic "1" to a logic "0" cell, VL1 is approximately VGS (M23). After the write "1" operation, the voltage VL1 at the drain of the transistor M26 reduces in value.

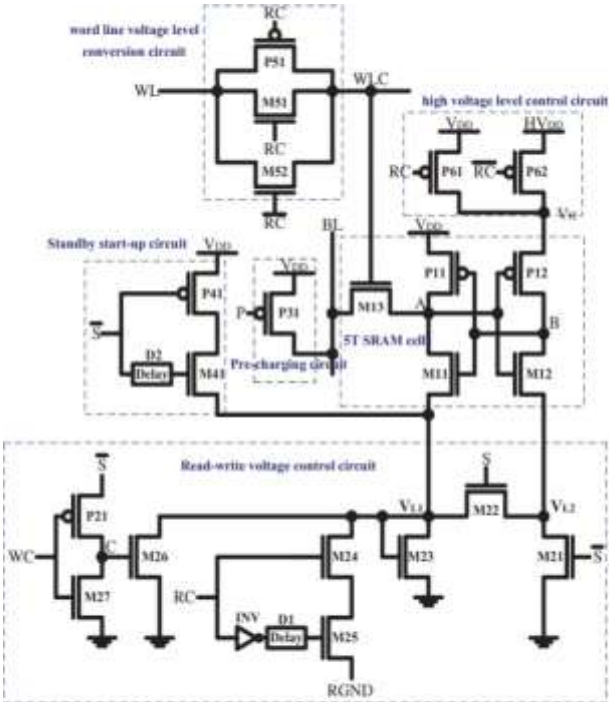

Figure 2 Circuit diagram of the proposed 5T SRAM cell.

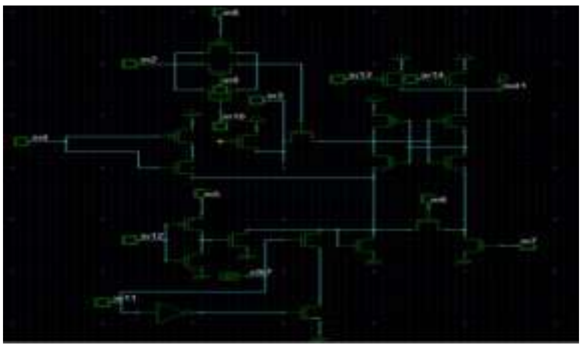

Figure 3 Proposed 5T SRAM cell.

TABLE I. THE OPERATING CONDITIONS UNDER DIFFERENT OPERATING MODES

RC	WC	S	V_{L1}	V_{L2}	mode
RGND	V_{DD}	0	$V_{GS(M23)}$	0	write
V_{DD}	0	0	RGND (1st phase) 0 (2nd phase)	0	read
RGND	0	V_{DD}	$V_{GS(M23)}$	$V_{GS(M23)}$	standby
RGND	0	0	0	0	hold

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C. 2- Phase Read Operation

The read operation utilizes a two-stage reading methodology to allow for high-speed reading and minimize unnecessary consumption of power. In the first stage of reading, since The voltage VL1 would be pulled down to a negative value RGND if transistor M25 were to continue conduction. The negative voltage RGND would, in this case, allow a proper increase of the reading speed.
On the other hand, transistor M24 remains on throughout the entire second read phase when the read control signal RC is logic high. Due to transistor M25 not being on in the sequel, the voltage VL1 is dropped down to ground potential, and thus power dissipation is minimized. It is worth mentioning that transistor M26 is always on, either in It can be seen that for effectively decreasing half- selected cell disturbance as well as leakage current, during reading a logic "1" operation, the absolute value of voltage RGND can be adjusted to be less than voltage VTM11.

Now consider reading as a "0" logic operation. As transistor M13 is on, and the voltage VWLC is VDD-VTM51, the first transient voltage at node A must be less than transistor M12's threshold voltage îVTM12Īįġ. Noting that the absolute value of the voltage RGND is stated to be lower than the voltage VTM11, it's meant to be less than the ground voltage.

D. Standby Operation

The regenerative feedback causes a data bit to flip when the voltage reaches some threshold value specific to that bit. The issue of writing "1" in the standard 5T SRAM cell is thus overcome with the completion of "1". The voltage VL1 is VGS(M23) when a written logic "0" becomes a logic "1." Upon completion of the "1" writing procedure, the voltage VL1 exiting the transistor M26 will eventually drop. M41 turns on while M21 enters full off as an activation signal S is assumed to be high. The equaliser is M22 regulated by the standby control signal S. As a result of M22 being ON, the VL1 and VL2 values of the later stages equal the VTM23. It must be noted that during dating this first standby cycle, M41 remains in the ON state. Consequently, the standby efficiency turns up since it takes little time before VL1 charges to VTM23.

IV. SIMULATION RESULTS AND DISCUSSION

To evaluate performance, this paper provides various structures of SRAM cells which were simulated under 90nm CMOS technology. All simulations were run at standard settings of room temperature and VDD=1.2V. Figure 3 shows a simulated waveform of a standard 5T SRAM cell that was unable to write a '1'. Figure 4 shows a waveform simulation of a successful write to the proposed 5T SRAM cell. The proposed 5T SRAM cell is obviously easier to write a logic '1' to the SRAM cell.

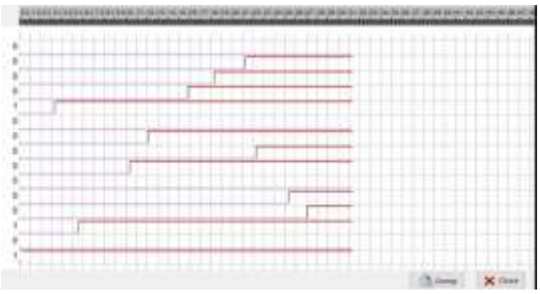


Fig 4 Timing Diagram

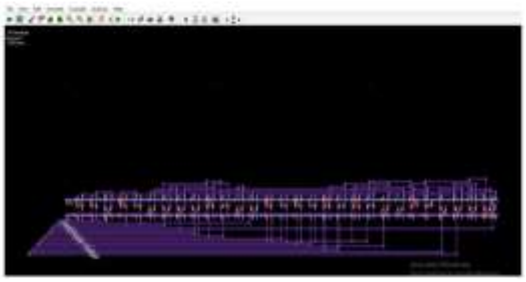


Fig 5 Schematic diagram

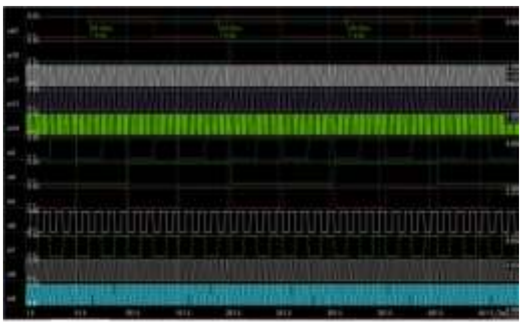
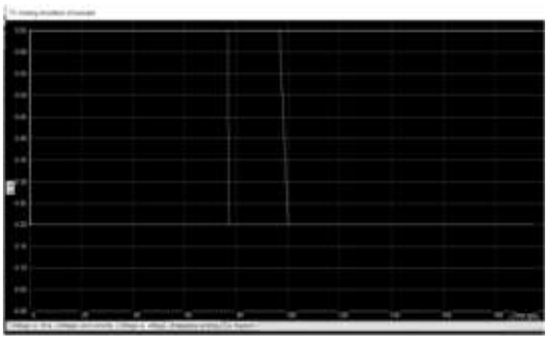


Fig. 6



Simulation wave form 5T SRAM cell

Fig. 7 Voltage and Currents

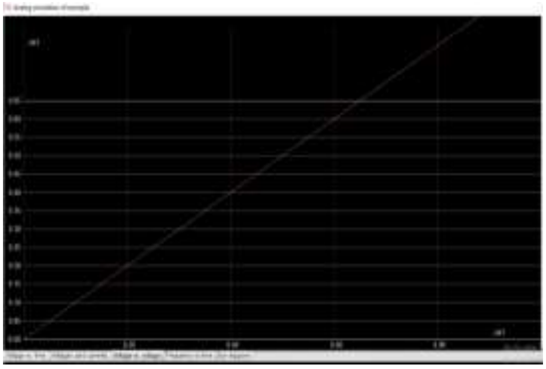


Fig. 8 Voltage vs Voltage

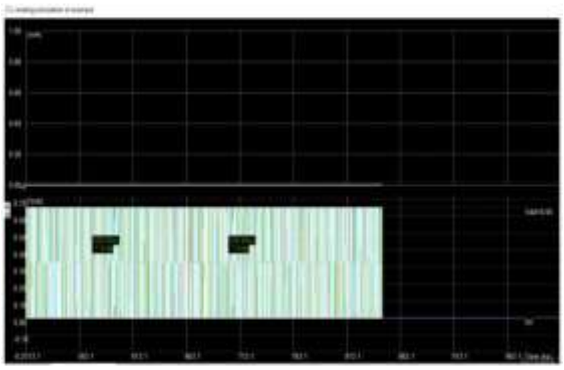


Fig 9 Frequency vs Time

Fig 10 Voltage level wave forms a read operation.

TABLE II: Reading Speed Comparison under Different Supply Voltages

Supply voltage (V)	Conventional 5T SRAM (ns)	Proposed 5T SRAM (ns)	Improving (%)
1.15	0.1213	0.0745	38.6
1.1	0.1537	0.1036	32.6
1.05	0.1993	0.1318	33.9

To evaluate performance, this paper provides various structures of SRAM cells which were simulated under 90nm CMOS technology. All simulations were run at standard settings of room temperature and VDD=1.2V. Figure 3 shows a simulated waveform of a standard 5T SRAM cell that was unable to write a '1'. Figure 4 shows a waveform simulation of a successful write to the proposed 5T SRAM cell. The proposed 5T SRAM cell is obviously easier to write a logic '1' to the SRAM cell.In the standby state, the supply voltage VDD is expressed in terms of voltage VBL, the ground status is designated by voltage VWL, and voltage VA maintains steady status at VTM23. In so doing, VGS for transistor M13 becomes less than the ground voltage. This is compared with the last case in which as illustrated, transistor MA1 will have zero VGS, that is, from one. To a larger extent, GIDL significantly lowers the current leakage across transistor M13 compared to transistor MA1. Drain-source voltage VDS of transistor M13 is now VDD-VTM23, while the supply voltage VDD is drain-source voltage VDS for transistor MA1. By virtue of the DIBL effect, the drain- source voltage VDS.

TABLE III: Leakage Current Comparison under Different Corner Model

Corner model	Proposed 5T SRAM (pA)	Conventional 5T SRAM (pA)	Improvement (%)
TT	11.5769	27.4534	57.8
SS	9.8987	13.5493	26.9
FF	49.8341	342.5346	85.5

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It is evident that the proposed 5T single- port SRAM is less leaky than a standard 5T SRAM. Finally, across all corner types, the standby leakage current from the proposal presented here is larger than that of a standard 5T SRAM cell by 57.8%, 26.9%, and 85.5%.

V. CONCLUSION

In this work, a highly efficient SRAM cell is introduced. The research presents three major contributions as (1) to develop a method to perform the write "1" operation without disabling the read operation; (2) to develop a read operation that has a high speed; and (3) to drastically reduce the standby current. It achieves allowing the write of a logic "1" to the cell, and simulation results also show very clear performance gains over the standard 5T SRAM cell. The speed-up for various supply voltages was 38.6%, 32.6%, and 33.9% with a two-phase reading method for speed-up of the reading. In comparison to the standard 5T SRAM cell, the proposed SRAM cell has standby leakage reduced by 57.8%, 26.9%, and 85.5%, respectively, in various corners.

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