2581-4575

International Journal For Recent Developments in Science & Technology

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IMPROVED SPEED AND POWER ANALYSIS ON HYBRID APPROXIMATE ADDERS USING 8:3-9:4 with 4:3, 3:2 COMPRESSORS.

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ABSTRACT

Multiplier is the key element in the digital and high performance systems such as FIR filters, digital processors and microprocessors etc. Most of the arithmetic operations are done using multipliers. Designing multipliers for the high –speed integrated circuit with low power consumption is today's major concern for the VLSI field. Among the existing multiplier, Wallace tree multiplier is popular multiplier architecture. Wallace tree multiplier is a parallel multiplier, hence faster than an array multiplier. Speed of conventional Wallace tree multiplier can be further improved by using compressors. The target is achieved by making use of 8:4, with 4:3 and 3:2 compressor techniques. In this paper, two numbers of 16-bits each are multiplied using Wallace tree multiplier. Performance analysis in terms of power, delay and power-delay product. The multiplier was implemented at the front end design using mentor graphics tool and Xilinx 14.2.

Keywords: Compressors,partial product generation,Wallace tree, FIR filters.

INTRODUCTION

Multiplication operation serves as the back bone of all signal processing applications like in DSP & Embedded systems. The speed of multiplier decides the speed of the processor. Speed attribute of any processor which involves multipliers depends on efficiency obtained in the multiplication process. Multiplication process can be stated as repeated sum of partial products. The final product is obtained by repeatedly adding the multiplicand to itself number of times specified by another multiplier. The hardware requirements of multipliers are very high which results in low precision, increase in chip area & hardware complexity along with increased latency. To carry out time efficient multiplication, high-speed multipliers are being used that electronically computes the result by following certain logics. Due to the vast application area of multipliers, it is imperious to design a multiplier that offers low latency, consumes low power

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along with physically compact design. Multiplication is intrinsically a three step process

- •partial product generation
- •partial product reduction
- •final result computation.

As the number of bits (to be multiplied) increases the number of partial products generated also increases. However, the problem comes while multiplying high order bits as the partial products reduction have long vertical paths which leads to high latency. The most common technique used by the designers to reduce these vertical paths was by using adders. More number of stages were introduced to reduce the partial products which eventually create problems such as signal discontinuities. So the designers come up with the idea of using compressors in multipliers. Compressors serve as a critical component of a multiplier & are used in large numbers to perform the reduction process. These are combinatorial devices that provide effective partial product reduction by reducing the latency of this step by following certain logics. The performance of the multiplier can be enhanced by improving the compressor designs by lowering the transistors count that ultimately reduces the delay. A compressor takes equally weighted inputs & produces binary outputs. More specifically a ***m:n*** compressor counts the number of ones at the inputs & provides with the binary count at the output (here m represents input bits & n represents output bits). The weight of the LSB of the compressor output is the same as the weight of each of the inputs, and the remaining bits have increasingly higher weights. Depending on the bits converted, compressors are classified into two classes low order compressors (such as 3-2, 4-2, 5-2) [3] & high order compressors (such as 5-3, 6-3, 7-3, 8-4, 9-4).In this paper, two designs of high order compressor (8-4 & 9-4) one using half & full adders& other using multiplexers are being designed& analyzed& their performance matrices such as power, delay & area are compared with the present technical designs.

Record The opening between capacities of CMOS improvement scaling and requirements of destiny utility terrific duties to hand is developing swiftly. There are more than one promising arrangement approaches that together can reduce this commencing internal and out. Evaluated figuring is one in all them and starting late, has pulled within the maximum grounded idea of preferred scientists. Induced figuring abuses natural bumble fine of employments and capabilities generic imperativeness useful programming and hardware usage by trading off computational great (e.G., precision) for computational undertakings (e.G., execution and essentialness). Consistently, multiple studies attempts have explored estimated preparing throughout every one of the layers of enrolling stack, regardless, maximum by way of a ways of the work at hardware stage of thought has been proposed on adders. In [1], a relative

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audit of leading edge unsightly adders is given. Additionally, it in like way offers examination in light of each popular association estimations and what's more evaluated enrolling layout estimations.

Harsh Compressors for Multiplication

Harsh figuring is an interesting attitude for reducing facet getting prepared at nanometric scales. Erroneous figuring is especially entrancing for PC calculating plans. The examination and plan of two new triggered four-2 blowers are cleared up in [2] to be used in a multiplier. These designs depend upon distinctive features of weight, to any such degree, to the point that imprecision in computation (as evaluated by the screw up charge and the affirmed institutionalized misstep expel) can meet regarding circuit-based totally figures of estimation of a blueprint (variety of transistors, deferral and power use). Four one in every of a kind gets equipped for using the proposed deduced blowers are proposed and separated for a Dadda multiplier [2]. Expansive entertainment consequences are given and a use of the collected multipliers to picture making plans is supplied.

The consequences show that the proposed traces accomplish essential abatements in control diffusing, deferral and transistor take a look at stood out from a right association; furthermore, two of the proposed multiplier designs provide brilliant capacities to photo duplication with admire to everyday institutionalized botch division and zenith motion to-uproar extent (extra than 50dB for the considered image outlines).

Unpleasant Wallace-Booth Multiplier

Unpleasant or obscure enrolling has starting overdue pulled in noteworthy idea in light of its capacity functions of enthusiasm with respect to unmatched and low electricity usage. This prompted multiplier [3] includes an expected Booth encoder, a indistinct 4-2 blower and an unpleasant tree shape. The ugly association is finished and affirmed for 8x8, 16x16 and 32x32-piece checked increment designs concentrating on applications in embedded structures. Reenactment consequences at 45 nm advancement are given and analyzed. Differentiated and a proper Wallace-Booth multiplier and moreover other deduced multipliers located in the precise written work, the proposed assessed scheme achieves basic enhancements in control use, postpone and united estimations. These outcomes display the commonplace experience of the proposed plan.

4:2 varieties of harsh multipliers

Harsh figuring can lessen the blueprint multifaceted nature with an extension in execution and energy functionality for screw up adaptable applications. Another arrangement method for gauge of multipliers is mentioned in [4]. The inadequate aftereffects of the multiplier are modified to display fluctuating possibility phrases. Basis multifaceted nature of estimation is vacillated for the overall of modified midway things in attitude in their probability. The proposed estimation is

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utilized in two forms of sixteen-bit multipliers. Amalgamation results screen that proposed multipliers achieve manipulate keep property of seventy two% and 38%, independently, seemed in a different way in relation to a right multiplier. They have higher precision while regarded in a different way on the subject of existing unsightly multipliers.

Execution of the proposed multipliers is surveyed with a picture dealing with utility, wherein one of the proposed fashions achieves the maximum hoisted zenith banner to upheaval quantity.

The want to help extraordinary digital banner managing (DSP) and collecting programs on essentialness obliged contraptions has reliably created. Such programs automatically typically carry out go segment enlargements the use of settled point calculating whilst inside the meantime showing flexibility for a few computational oversights. Hence, improving the essentialness capability of increments is essential. Finally, the confirmed computational bungle [5] does not make any unmistakable effect at the concept of DSP and the precision of request packages.

PROPSOED HYBRID METHOD

Two designs are presented to design 8-4 & 9-4 compressors are combined to for 17:8 compressor using HDL designer series. The first design is by using adders & another design is by using multiplexers. Both the high order compressor's designs show

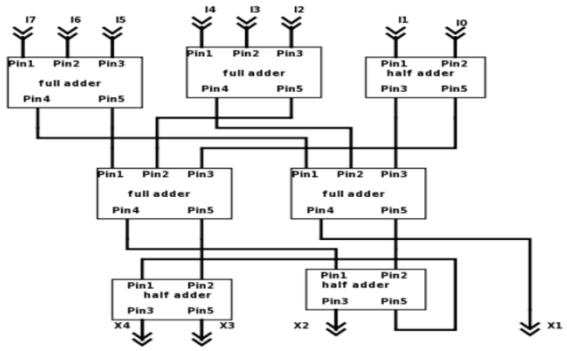

Figure 1 shows the schematic of 8-4 compressor designed using half adders & full adders.

An 8-4 compressor has eight inputs (i0-i7) & produces four outputs (X1-X4) i.e.it compresses eight partial products into four. If all the input bits are one (i.e.11111111), then the output will be 1000. It demonstrates that output is the binary equivalent of the inputs. It uses three stages of half & full adders to compress the inputs by applying all sum outputs of the first stage to one adder of the second stage & all carry outputs to another adder. The set of equations (1-4) shown below governs the process.

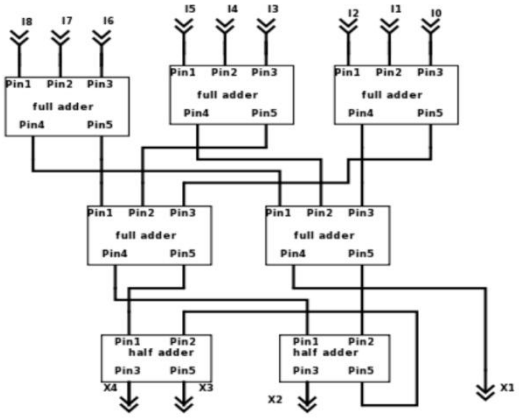

Figure 2 shows the schematic ofthe9-4compressor using three stages of adders.

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It takes nine inputs (I0-I8) & compresses to 4 outputs (X1-X4) following a set of equations (5-8). In 9-4 compressors, if all the inputs are high i.e.I0-I8 are high (11111111) then maximum output (X1-X4) will be 1001. The proposed 9-4 compressor uses a combination of 5full adders &half adders. The total number of adders used in the proposed design are much less as compared to the number of adders used in low order compressors as in low order, the number of components increases progressively with the input bits to be compressed. So the number of stages decides the performance characteristics such as delay, area, power consumption.

SIMULATION RESULTS

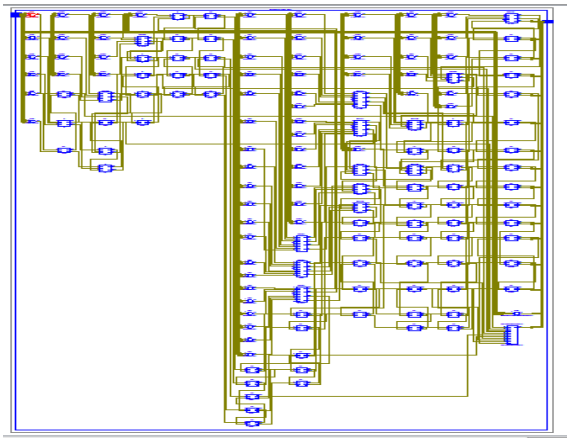

Figure 4 RTL Schematic

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	88	960	9%
Number of 4 input LUTs	155	1920	8%
Number of bonded IOBs	32	108	29%

Figure 5 Design Summary

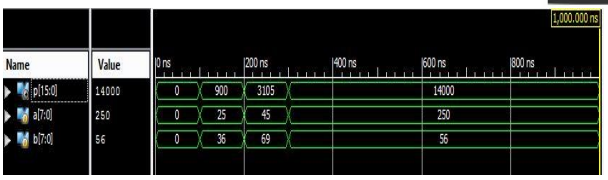

Figure 6.Approximate Multiplier output

CONCLUSION

In the current design scenario, a 8*8 Wallace tree multiplier using compressors based on full adder was designed HDL designer series and Xilinx Tool. Wallace tree Multiplier using compressors are better than the conventional Wallace tree multiplier in terms of speed

FUTURE SCOPE

Redundant basis (RB) multipliers over Galois Field have gained huge popularity in elliptic curve cryptography (ECC) mainly because of their negligible hardware cost for squaring and higher order approximate addition and multipliers

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