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IMPLEMENTATION OF THREE-PHASE SOLAR P V INTEGRATED UPQC

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Abstract: This paper deals with the design and performance analysis of a three-phase single stage solar photovoltaic integrated unified power quality conditioner (PV-UPQC). The PV-UPQC consists of a shunt and series connected voltage compensators connected back to back with common DC-link.The shunt compensator performs the dual function of extracting power from PV array apart from compensating for load current harmonics. An improved synchronous reference frame control based on moving average filter is used for extraction of load active current component for improved performance of the PVUPQC. The series compensator compensates for the grid side power quality problems such as grid voltage sags/swells. The compensator injects voltage in-phase/out of phase with point of common coupling (PCC) voltage during sag and swell conditions respectively. The proposed system combines both the benefits of clean energy generation along with improving power quality. The steady state and dynamic performance of the system are evaluated by simulating in Matlab-Simulink under a nonlinear load. The system performance is then verified using a scaled down laboratory prototype under a number of disturbances such as load unbalancing, PCC voltage sags/swells and irradiation variation.

INTRODUCTION

There is an increasing need for renewable energy systems with ancillary features particularly in low voltage distribution systems. This is due to the fact that there is an increased penetration of nonlinear power electronics based loads and renewable energy based systems [1]–[3]. These power electronic loads though energy efficient, inject harmonic currents into grid which cause distortion at point of common coupling (PCC) particularly in weak grid systems. Moreover, these power electronic loads are sensitive to disturbances in voltages. In weak distribution systems, due to the intermittent nature of the clean energy sources such as wind and solar energy, their increased penetration leads to PCC voltage fluctuations depending upon power generation and demand. These voltage fluctuations can affect sensitive power electronic loads such as adjustable speed drives, lighting systems etc which can lead to frequent tripping, maloperation and thus leading to increased maintenance costs.

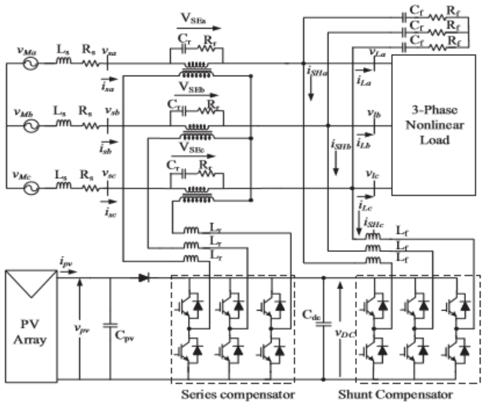


Fig. 1. System Configuration PV-UPQ

Renewable energy integration with power quality enhancing systems such as dynamic voltage restorer (DVR), unified power quality conditioner (UPQC) and distribution static compensator (DSTATCOM) provides an ideal solution by combining benefits of clean energy with power quality enhancement. Most of the research on renewable energy system with power quality improvement has been carried out in case of shunt voltge source converter (VSC) based systems. A solar PV integrated shunt VSC with DSTATCOM functionalities such as grid current power quality improvement has been proposed in [4], [5]. A novel toplogy of PV and DVR systems with reduced number of switches has been proposed in [6]. Though DSTATCOM can also perform voltage regulation, it comes at the cost drawing reactive power from the PCC. Moreover, DSTATCOM cannot protect load from harmonics in PCC voltage. UPQC with its series and shunt VSCs, provides both load voltage regulation as well as improvement in grid current quality. UPQC provides a complete solution for mitigating both the load side and PCC side power quality issues [7].

2.CONFIGURATION OF PV-UPQC-S

The topology of a PV-UPQC-S is presented in Fig. 1.4. The major parts of the system are a series VSC and shunt VSC connected back to back through a common DC-bus. The VSCs are connected to PCC using interfacing inductors. Ripple filters are used to filter out switching harmonics of the VSCs. The series VSC injects voltage through a series injection transformer. The PV array is connected directly at the DC-bus of UPQC through a reverse blocking diode.

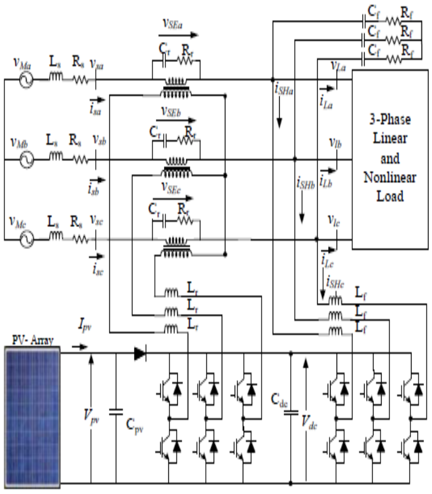


Fig: 2. Structure of PV-UPQC-S

The phasor diagram of the PV-UPQC-S with a linear reactive load is presented in Fig. 1.5. The subscript ’1’ represents condition when reactive power is shared by shunt VSC only whereas the subscript ’2’ refers to condition when the series VSC shares a part of reactive load power. The PCC voltage ($VS1$) and load voltage ($VL1$) are in phase when series VSC is not injecting any voltage. The load current before series compensation is (*IL*1) and the load angle is (φ).

The shunt VSC also injects real power obtained from PV array which is represented by (*IPV*). The remaining part of the load real power is obtained from the grid (*IS*1). The shunt VSC current (*ISH*1) before series VSC injection is phasor sum of PV array current and load reactive current.

When a part of reactive power of the load is to be shared by series VSC, then series VSC injects voltage (*VSE*) such that load voltage is shifted to (*VL*2). This results in shifting of load current to (*IL*2). However, as the active current drawn from the grid is to remain same (*IS*1 = *IS*2 = *IS*), the shunt VSC current reduces to (*ISH*2). It can observed that due to power angle (δ), the part of reactive burden of shunt VSC is shared by the series VSC thus increasing the utilization of series VSC

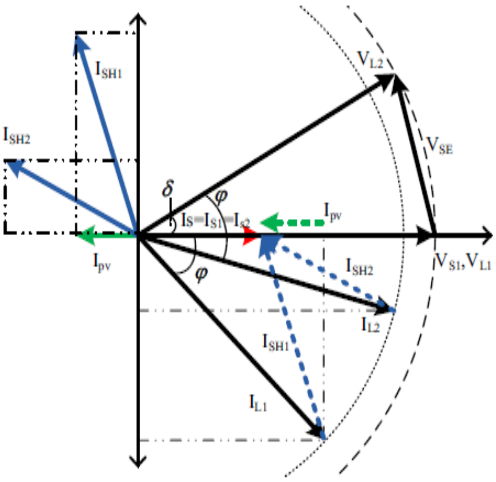


Fig: 3 Phasor Diagram of PV-UPQC-S

For a given reactive power sharing by series VSC, the magnitude of series VSC voltage *VSE* is lesser under sag condition as compared to swell condition. This is because the grid current *IS* is higher under sag condition as compared to swell condition for a constant load. Based on these observations, in order to prevent excessive VA rating of series VSC, the control implemented is such that, it compensates for reactive power under sag and nominal conditions. The PV array is designed such that it supplies around 30% of load active power. This is because as more load active power is supplied by the PV array, there is less current drawn from the grid which reduces the reactive power sharing capability of series VSC for a fixed voltage rating of series VSC. The complete design parameters of PV-UPQC-S.

3. CONTROL OF PV-UPQC-S

There are four control blocks involved in the control of PVUPQC- S. These are GCDSC block, load power calculation block, shunt VSC and series VSC control block. These are elaborated as follows:

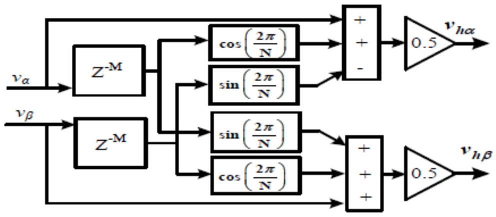
3.1 Generalized Cascaded Delay Signal Cancellation Block

A delay signal cancellation (DSC) operator [22] for extraction of FFPS component of voltage is given as,

$$v_{h\alpha-\beta}(t)=\frac{1}{2}\left[v_{\alpha-\beta}(t)+e^{j\frac{2\pi}{N}}v_{\alpha-\beta}\left(t-\frac{T}{N}\right)\right] \qquad (1)$$

Where $v\alpha-\beta(t) = v\alpha + jv\beta(t)$ is the voltage vector in α, β frame, $vh\alpha-\beta(t) = vh\alpha(t) + jvh\beta(t)$ is the FFPS component of voltage along with harmonics of order $h = N \times k+1$ ($k = \pm1,\pm2,\pm3\ldots$) in $\alpha-\beta$ domain, T is the fundamental period of voltage, N is the delay factor. The transfer function of DSC operator is given as,

$$G_N(j\omega) = \left|\cos\left(\frac{\omega T}{2N}-\frac{\pi}{N}\right)\right| \angle -\left(\frac{\omega T}{2N}-\frac{\pi}{N}\right) \qquad (2)$$



(a) Delay Signal Cancellation Block-N

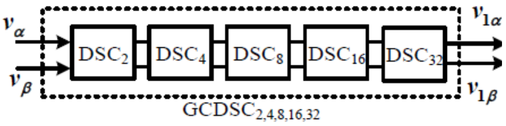


Fig: 4. Fundamental Frequency Positive Sequence Extraction using Generalized Cascaded Delay Signal operation

A delay factor N blocks harmonics of the order $hb = N \times k - 1$ ($k = \pm1,\pm2,\pm3...$). The mathematical implementation of DSC operator is presented in Fig. 3.3(a). As it can be observed from the figure, in discrete form, the delay is implemented by $z{-}M$ where M is delay samples corresponding to a delay factor of N. When the harmonic content of PCC voltage is unknown, it is often recommended to cascade five delay signal operator blocks with delay factors N = 2, 4, 8, 16, 32. This system of cascaded blocks is known as GCDSC block as represented in Fig. 1.6(b).

The system can be made frequency adaptive, by using GCDSC block as a prefiltering scheme as in case of GCDSCPLL [22]. When the GDSC is designed for a frequency of 50Hz, a signal of 49Hz is attenuated by 0.065% and phase error of 3.43◦ as it can be obtained from (2). Since the normal grid fundamental frequency variation is from 49.3 to 50.2 Hz [26], this variation causes only negligible magnitude and phase error. Hence, frequency adaptation can be avoided to prevent unnecessary complexity in the system.

The magnitude response of GCDSC is shown in Fig. 1.7. The frequency axis in the plot is normalized with respect to 50Hz frequency. It can be seen that GCDSC allows only FFPS components and substantially attenuates lower order harmonics. However, certain harmonics which are expressed as $h = 32 \times k + 1$, ($k = \pm1,\pm2..$) are passed without attenuation (i.e 33*rd* positive sequence harmonic, 31*st* negative sequence harmonic etc.). Normally, the magnitude of such components are negligible. However, they can still cause error in calculation of phase and magnitude information. Hence a band-pass filter (BPF) is also used to remove these high frequency signals from FFPS signal obtained using GCDSC.

4. SIMULATED PERFORMANCE

The dynamic behavior PV-UPQC-S under dynamic conditions is simulated in Matlab/Simulink software using SimPowerSystems blockset. The dynamic performance is evaluated at different conditions such as fluctuation in PCC voltages, irradiation variation and load unbalance conditions. The load used is a combination of linear and nonlinear loads.

A. PV-UPQC-S Performance Under Load Unbalance Condition

The PV-UPQC-S performance during load unbalance condition is presented in Fig.2.1 The signals shown are PCC voltages (vs), load voltages (vL), DC-bus voltage (Vdc), grid currents (is), load currents (iL), shunt VSC currents (iSH), PV array power (Ppv). At 0.51 s the phase ’b’ of load is disconnected thus resulting in an unbalanced nonlinear load. It can be observed that the shunt VSC of PV-UPQC-S maintains the grid currents balanced at unity power factor. The DC-bus voltage settles within 0.04 s to its regulated value of 700 V after a slight overshoot of 20 V.

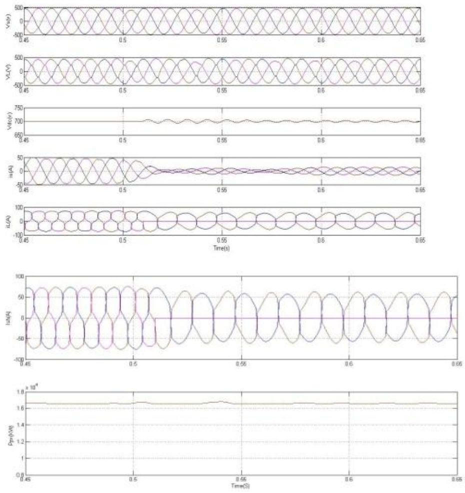


Fig.5. PV-UPQC-S Performance Under Load Unbalance Condition

B. PV-UPQC-S Behavior during Irradiation Change

The PV-UPQC-S performance during change in irradiation is presented in Fig.2.2. The signals shown are PCC voltages (vs), load voltages (vL), DC-bus voltage (Vdc), grid currents (is), load currents (iL) of phase ’a’, shunt VSC currents (iSH) of phase’a’, PV array power (Ppv), series VSC voltages (vSE) and power angle (δ). From 0.95s to 1 s the solar irradiation is varied from 1000 $W/m2$ to 500 $W/m2$. As it can be observed from Fig. 9, the power angle and series VSC voltages are higher at higher PV power as compared to lower PV power. This is due the fact that, as the PV array power supplies a part of load real power demand, the grid current drawn is lower. Hence, to compensate the same reactive power, the load angle and series VSC voltage is higher as compared to case when the PV array power is lesser.

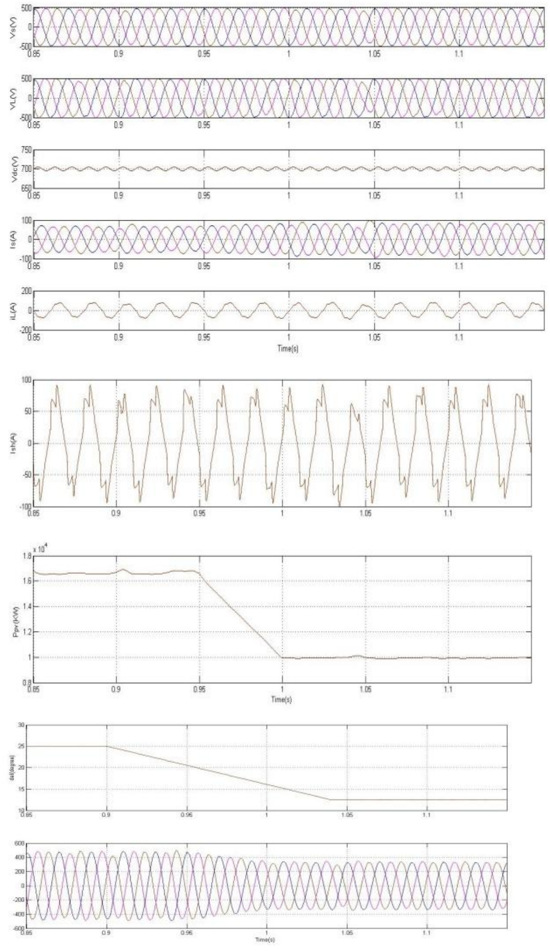


Fig.6. PV-UPQC-S Behavior during Irradiation Change

C. PV-UPQC-S Performance during PCC Voltage Disturbances

The PV-UPQC-S behavior under PCC voltage disturbance is presented in Fig.2.3. The solar irradiation (G) is keptconstant at 1000 *W/m*2. The signals shown are PCC voltage of phase ’a’ (*vs*), load voltages (*vL*), DC-bus voltage (*Vdc*), grid currents (*is*), load current (*iL*), shunt VSC current (*iSH*), PV array power (*Ppv*), power angle (*δ*), series VSC voltages (*vSE*). Only signals of one phase are shown in case of certain signals for clarity in representation. At 0.65 s, there is a voltage sag of 0.3 pu along with harmonic distortion and at 0.75 s there is voltage swell of 0.3 pu along with harmonic distortion. It can be seen that load voltage is sinusoidal and reference value despite the distortions in PCC voltage. Under nominal conditions, as seen from *δ* and *vSE* the series VSC still operates to share a part of reactive power of the load. Under swell conditions, the series VSC compensates only swell and no reactive power sharing is done, which is shown by *δ* being zero under voltage swell. After PCC voltage swell, there is a slight delay of 2 cycles for series VSC to calculate necessary

power angles. This is due to low pass filters using in *PL* and *QL* calculation.

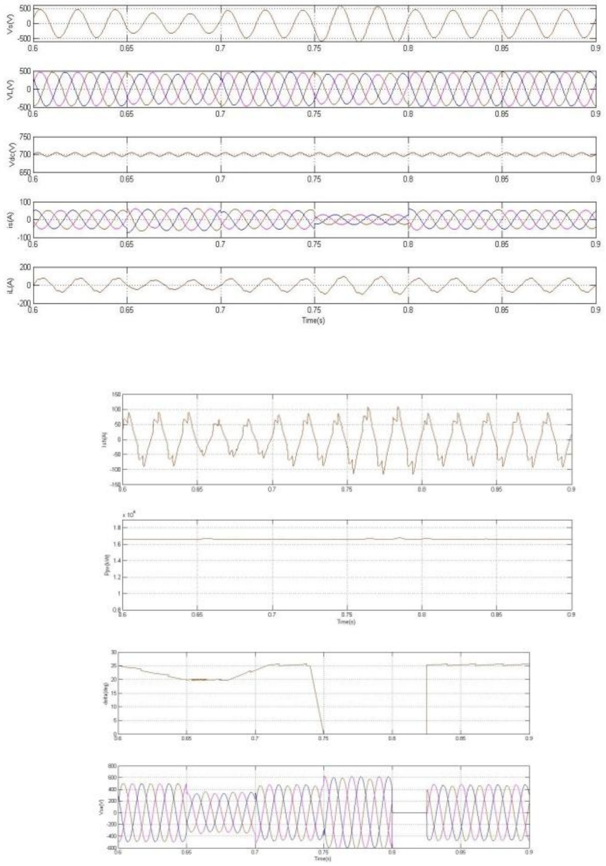
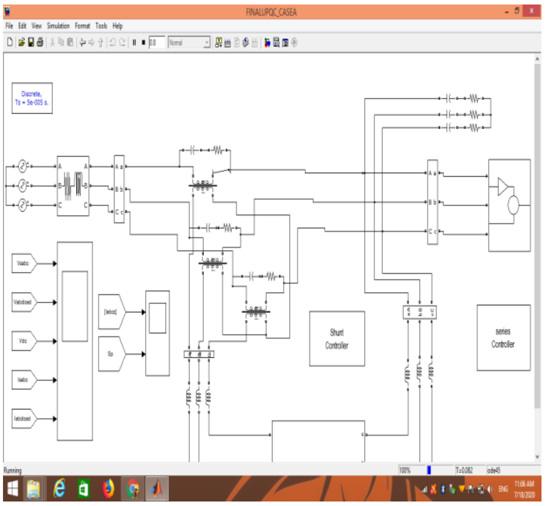
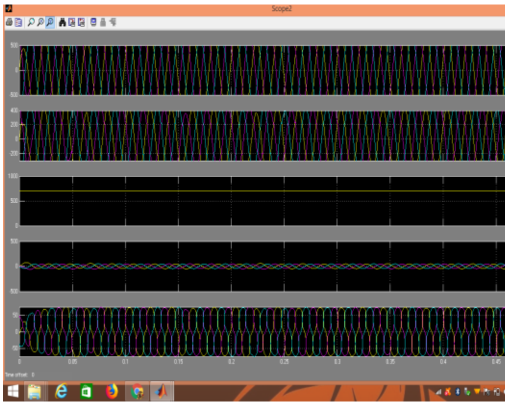


Fig.7. PV-UPQC-S Performance during PCC Voltage Disturbances

5.RESULTS





Nodal Voltage vs Time

6. CONCLUSION

The design and dynamic performance of three-phase PVUPQC have been analyzed under conditions of variable irradiation and grid voltage sags/swells. The performance of the system has been validated through experimentation on scaled down laboratory prototype. It is observed that PVUPQC mitigates the harmonics caused by nonlinear load and maintains the THD of grid current under limits of IEEE-519 standard. The system is found to be stable under variation of irradiation, voltage sags/swell and load unbalance. The performance of d-q control particularly in load unbalanced condition has been improved through the use of moving average filter. It can be seen that PV-UPQC is a good solution for modern distribution system by integrating distributed generation with power quality improvement.

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