2581-4575
International Journal For Recent Developments in Science & Technology
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CHARACTERIZATION OF THERMAL/FLOW CHARACTERIZATION OF THERMAL INTERFACE MATERIALS

GUNDA DINESH, DR.V.ASHOK KUMAR, A. KRISHNA

PG Scholar Department of Mechanical Engineering, Mother Theressa College of Engineering & Technology

Associate professor & HOD Department of Mechanical Engineering, Mother Theressa College of Engineering & Technology

Assistant Professor Department of Mechanical Engineering, Mother Theressa College of Engineering & Technology

ABSTRACT

In this paper new characterization equipment for thermal interface materials is presented. Thermal management of electronic products relies on the effective dissipation of heat. This can be achieved by the optimization of the system design with the help of simulation methods. The precision of these models relies also on the used material data. For the determination of this data an experimental set-up for a static measurement is presented, which evaluates thermal conductivity and interface resistance of thermal interface materials (e.g. adhesive, solder, pads, or pastes). A qualitative structure-property correlation is proposed taking into account particle size, filler content and void formation at the interface based on high resolution FIB imaging.

The paper gives an overview over the set-up and the measurement technique and discusses experimental and simulation results.

1. INTRODUCTION

It is common practice for high power applications to assemble power devices as bare dies in chip on board technique or to use flip chip assemblies with a directly mounted copper or aluminum heat sink. The thermal resistance (Rth) of the thermal interface material (TIM) is the bottleneck of the thermal heat flow from the active device junction to the cooler. All the more important is the fact of strongly localized hot spots, as heat spreading requires better thermal interface materials as just heattransfer [1, 2]. If possible, it is useful and common to reduce the thickness of the thermal interface material. But for thinner thermal interface materials the thermal interface resistance (between the silicon and the thermal interface material (Rth0,Si-TIM) as well as between the thermal interface material and the cooler material (Rth0,CM-TIM)) is no longer negligible [3, 4]. Therefore it is essential to account for this effect in the measurement set-up. In the system design process thermal simulation is used among other tools to select the thermal interface material to find the optimum situation. To build up the simulation model and get a suitable solution it is necessary to

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know the accurate geometry and material parameters. As , the trend is towards thinner thermal interface materials, the thermal interface resistances should be considered in the thermal simulation model. There are several standardized test methods (ASTM E 1225-99, ASTM E 1461-01, ASTM E 1530-99, DIN V 54462) as well as in-house-built and market going set-ups to determine the thermal resistance [5]. The most widely used methods are to place the thermal interface material between two plates, heating the top plate and cooling the bottom plate [6, 7, 8] or to use photo or laser flash set-ups [9]. In the paper different thermal interface materials (adhesives) are characterized varying different measurement and material parameters. Thus the thermal conductivity of the materials and the interface resistance is characterized. It is shown that the interface material can become a key issue for the thermal management of dynamically loaded devices. On this example a model with statically determined material data is validated and discussed in simulation and experiment.

2. THERMAL INTERFACE MATERIAL

Thermal Interface Materials as paste, pads , gels, adhesives or solders are used to fulfill the gap or tilt between to surfaces to optimize the thermal path between them. In microelectronics applications the adjacent materials are usually silicon and the heat sink materials Al or Cu. Figure 1 shows on the left hand side a typical power assembly application e.g. for a reverse-side cooled power device in flip-chip technology.

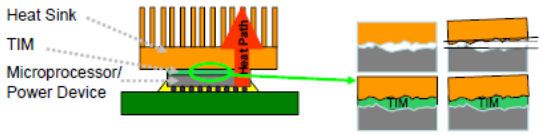

Fig. 1: Thermal interface material is used to fulfill the gap or tilt between to surfaces. For example, on the left a typical reverse-side cooling power assembly application is given.

3. TEST SET-UP

3.1. Structure

The idea to develop a new kind of set-up was to realize test conditions as they occur in real assemblies. That means using the same surface materials and assembly technology as in the real device instead of pellets made of adhesives (or solder).

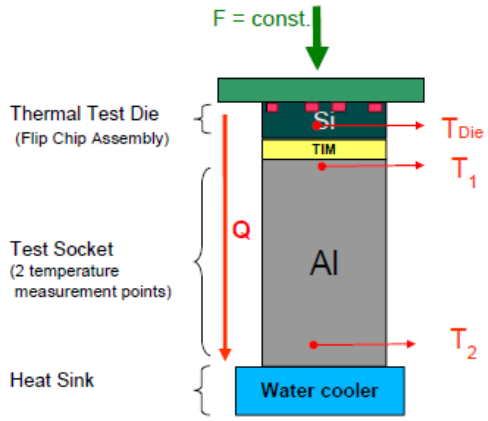

Fig. 2: Principle schematic for new test set-up

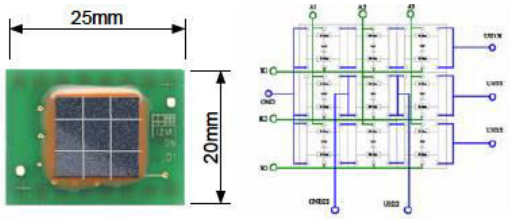

Fig. 3: Thermal test chip assembly and electrical interconnection schematic

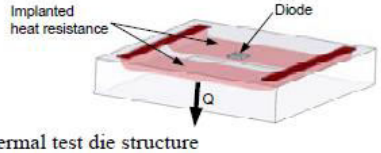

Fig. 4: Thermal test die structure

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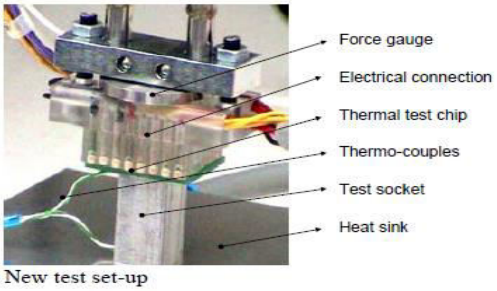

Fig. 5: New test set-up

Usually the determination of the heat flow through a thermal interface material is assumed to be equal to the electrical power loss. But there is a parallel heat flow through the electrical connection block. Radiation and free convection could be neglected as shown in section 3.3. Using the presented new assembly structure the real heat flow through the thermal interface material can be determined. Figure 6 derives the thermal equivalent circuit for the set-up.

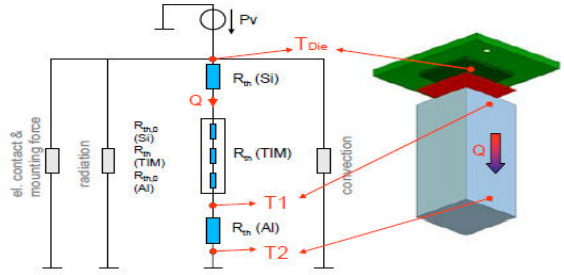

Fig. 6: Schematic of thermal equivalent circuit for test socket and test chip.

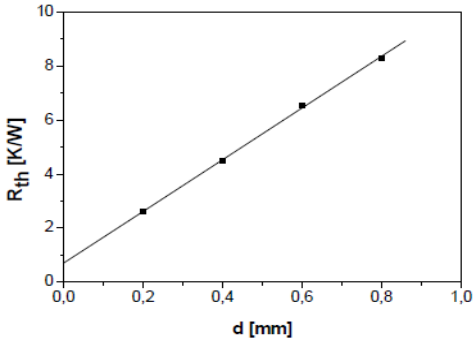

Fig. 7: Numerical linear fit through several measurements points of the same TIM with different thickness leads to the thermal conductivity of the TIM (k_{TIM}) and the sum of both thermal interface resistances ($R_{th0,Si\text{-}TIM}$ and $R_{th0,TIM\text{-}Al}$).

4. RESULTS

4.1. Measurements

Figure 8 shows the characteristics of four Ag-filled adhesives based on epoxy or modified epoxy bulk material.

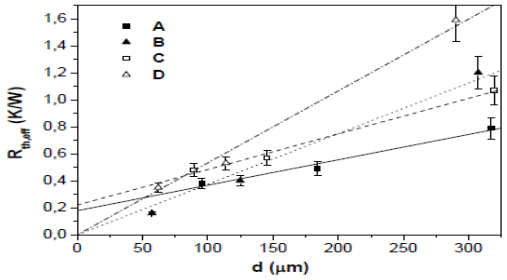

Fig. 8: Characteristic curves of four Ag- filled adhesives are used to determine its thermal conductivities and thermal interface resistances.

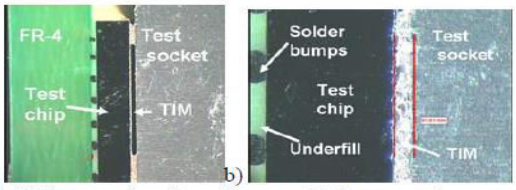

Fig. 9: Cross section of test chip assembled on test socket to determine the TIM thickness.

After numerical linear fitting, thermal conductivities and interface heat transfer coefficients could be determined (table 1).

Tab. 1: Determined parameters for investigated Ag filled Epoxy adhesives (A = 11,8 * 11,8 mm²).

Investigated adhesive types	k_{eff} (W/mK) (d = 100µm)	k_{TIM} (W/mK)	$2*R_{th0} * A$ (K cm²/ W)
A	1,9	3,8	0,24
B	2,5	1,9	0,07
C	1,4	2,7	0,31
D	1,3	1,3	0,014

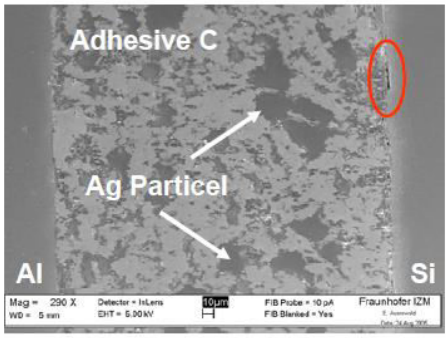

Fig. 10: Cross-section of TIM layer

Figure 11 shows a cut-out of figure 10 where in the boundary surface region pore structures would observed.

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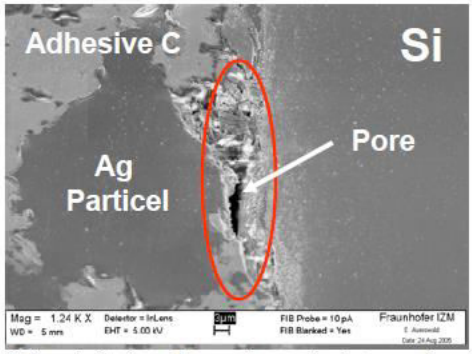

Fig. 11: Pore in the boundary surface region between the silicon chip and the Ag-filled copolymer TIM.

To have a better view into the depth of the interface, the boundary surface regions were analysed by focus ion beam (FIB) and SEM.

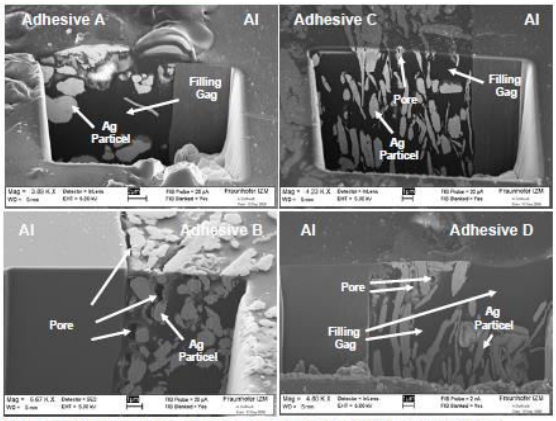

Fig. 12: Comparison of cross-sections for TIM-Si boundary section from Ag-filled adhesives .

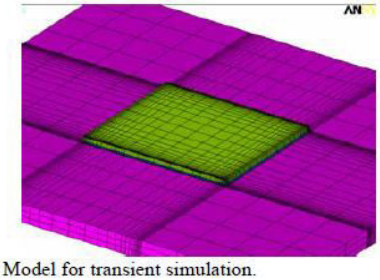

Fig. 13: Model for transient simulation.

Figure 13 shows the model structure. The chip is assembled on a FR-4 PCB. The die attach area is filled with thermal via's. Table 2 gives the model parameters.

Tab. 2: Model parameters for investigated transient thermal simulation.

A_{Chip} [mm²]	d_{Chip} [µm]	d_{TIM} [µm]	d_{PCB} [µm]	d_{CU} [µm]	th. via count	dia_{Via} [µm]
8 x 8	360	100	1600	70	100	500

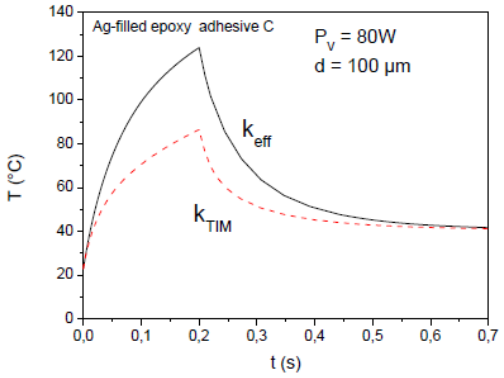

Fig. 14: Transient temperature behaviour in respect with and without considering the thermal interface resistances.

Figure 14 compares the transient behavior. As expected, the observed temperature rise for the solution of the model, considering only the thermal conductivity kTIM, is much less than considering the effective conductivity. That means that in real systems the junction temperature will be much higher as through simulation expected. This caused an over heating of the device and in the end its damage.

5. DISCUSSION OF RESULTS

The metallurgical results have shown that it is necessary to observe the TIM and its boundary regions. The Ag particles of adhesives B and D have for instance a closer contact between each other as the Ag particles of TIM A or C which results in a higher thermal bulk conductivity (c.f. figure 8). The observed filling gaps and pores in the bulk material could be a reason for the difference of thermal interface resistances for the investigated four adhesives. Especially if pores are close to the interface region, as seen in figure 11, the thermal interface resistance will be influenced. This is in correspondence with the measured results. TIM A and C have larger Ag

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particles as B and D and they show a better thermal conductivity because of its larger particle surface, which leads to less interfaces between the particles over the TIM thickness d thus enhancing heat transfer.

For thick TIM layers the effective thermal conductivity follows from the bulk resistance.

$$k_{eff}(d \to \infty) = k_{TIM} \qquad (Eq\ 11)$$

Figure 15 shows for the investigated TIMs the mentioned behaviour.

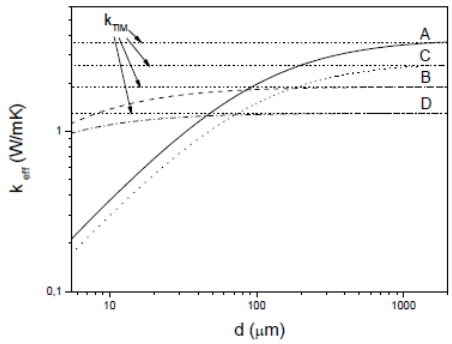

Fig. 15: Behavior of effective thermal conductivity in respect to the thickness for the investigated Ag-filled adhesives.

6. CONCLUSION

A new test set-up to characterize thermal interface materials was investigated. The novelty is that the set-up allows to measure all classes of TIMs (incl. solder and adhesive) under real assembly conditions.

The advantages are:

• High versatility (all TIM).

• A rapid test method using a test socket.

• An inexpensive method using standardized reference test socket material with narrow tolerances.

• Obtaining all relevant of information concerning: thickness, force, keff, kTIM, Rth0,i

• TIM thickness determination by crosssectioning.

• Design allows easy analysis by FIB and/or SEM

• Flip-chip assembly for thermal test chip used as to assure flatness of die (important for greases)

• Test uses surfaces as in real devices

• More accuracy is possible to improve temperature

measurement while using thermocouples with less measurement errors. The determination of thermal interface resistance and thermal conductivity was exemplified for four adhesives. The Structure of the adhesive was analyzed by FIB and SEM. It was found, that there is a structure-property correlation with respect to thermal properties. Voids, particle size and filler content could be shown to influence interface resistance and bulk conductivity and was explained accordingly. Also the influence of the thermal interface resistance was shown by thermal simulation.

7. REFERENCES

[1] S.V. Garimella, Y.K. Joshi, A. Bar-Cohen, R. Mahajan, K.C.
Toh, V.P. Baelmans, J. Lohan, B. Sammakia, and F. Andros.
'Thermal challenges in next generation electronic systems –
summary of panel presentations and discussions' IEEE Trans.
On Components and Packaging Technologies, 25(4):569–575,
2002.

[2] R. Viswanath, V. Wakharkar, A. Watwe and V. Lebonheur.
'Thermal Performance Requirements from Silicon to Systems',

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal

Intel Technology Journal Q3, pp. 1-16, 2000.
[3] Blazej, D. 'Thermal Interface materials', Electronics Cooling,
Volume 9, Number 3, August 2003, S. 14 ff
[4] Bruce M. 'Calculations for thermal interface materials';,
Electronics Cooling, Volume 9, Number 3, August 2003, S. 8 ff
[5] Lasance, C. J.M. 'Problems with Thermal Interface Material
Measurements: Suggestions for Improvement',
http://www.electronicscooling.
com/html/2003_november_a2.html
[6] Bosch, E., Lasance C. 'High accuracy thermal interface
resistance measurement using a transient method' Electronics
Cooling, Vol.6, No.3, September 2000
[7] Netzsch TCT416 ,
http://www.netzsch.de
[8]
http://www.thermagon.com/pdf/Resistance.pdf
[9] Wöstmann, F.-J, Hahn, O. 'Messverfahren zur Ermittlung
der Wärmeleitfähigkeit dünner Klebschichten', Produktion von
Leiterplatten und Systemen, Heft 1, S. 139ff, 2005
[10] May, D. 'Entwurf und Aufbau eines Messplatzes zur Charakterisierung
von Thermischen Interface Materialien', Diploma
Thesis, FHTW, Berlin, Germany, 2004
[11] Schacht, R., May, D., Wunderle, B., Gollhardt, A., Wittler,
O., Michel, B., Reichl, H. 'Characterization of Thermal Interface
Materials for Thermal Simulation', ESTC 06, Dresden,
Germany, 2006