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INTEGER SCALED TWO DIMENSIONAL DCT BASED OFDM

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ABSTRACT

The conventional OFDM system employs the IFFT-FFT structure to impart the orthogonality feature. However, due to complex nature of FFT, implementation size is large enough. The orthogonality can also be provided if IDCT-DCT structure is used in place of FFT. This will reduce the implementation area and will also increase the computation speed as only real calculations are required. In this paper we present the implementation of DCT based OFDM system. The DCT structure prevalent in H.264 standard is taken into reference as it has faster operation as compared to conventional DCT structure. The implementation of DCT-IDCT structure was done on ALTERA CYCLONE –II FPGA. The results show that the speed of calculation of orthogonal components is increased three folds while the implementation size reduces to half as compared to FFT based design.

Keywords: OFDM, FFT, 2D-DCT, BER, WLAN

1. INTRODUCTION

In many of the recent research works, as compared to Fast Fourier Transform based Orthogonal Frequency Division Multiplexing (FFT-OFDM), Discrete Cosine Transform – OFDM (DCT-OFDM) have been shown to be hardware efficient and particularly, for one-dimensional (1-D) modulations (real-valued modulation formats), such as BPSK and pulse amplitude modulation (PAM), in the absence of a quadrature modulator, DCT-OFDM can completely avoid the in-phase/quadrature-phase (IQ) imbalance problem addressed in [1] inherent in conventional DFT-based OFDM systems. Recently, it was shown analytically in [2] that in the presence of frequency offset, the ICI coefficients in DCT-MCM are more concentrated around the main coefficient (i.e., less ICI leakage to adjacent subcarriers) than in DFT-MCM. This results in better performance robustness to frequency offsets. The time selectivity can further be reduced if a smaller DCT size is used. However, this will reduce the spectral efficiency due to the need of larger cyclic prefix between each OFDM symbol to overcome ISI.

Two-dimensional (2D) fast Fourier transform (FFT) modulation for OFDM was introduced in [3] corresponding to a diversity transform in time domain [4] over 1D-FFT OFDM symbols. The actual 2D-FFT OFDM transmission was recently invented in [5] by introducing a 2D cyclic prefix (CP) to relay networks to facilitate semi-full-duplex

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operation and thereby increase the transmission rate with CDD.

The DCT basis is well known to have excellent spectral compaction and energy concentration properties. This, in turn, leads to improved performance with interpolation based channel estimation and can result in improved adaptive filtering convergence. The spectral performance of a 2D DCT is similar to the 1D case only with the exception that the minimum carrier spacing is further reduced. We can extend the basic 2D FFT OFDM theory to 2D DCT OFDM while keeping the pilot spacing and equalization parameters similar to 1D FFT OFDM. Although the bandwidth requirement will still be the same as conventional 1D FFT OFDM, the implementation cost and the BER performance will improve on the similar grounds as that of replacing 1D FFT OFDM by 1D DCT OFDM.

Few fast DCT algorithms proposed in [6] and [7] can provide fewer computational steps than FFT algorithms. This implementation however, does require, floating point computation which is not convenient for application which requires small design size.

Within still-image and video coding standards, such as JPEG and MPEG-1/2/4 [8], the DCT and its fast algorithm designs have been widely utilized for transformation coding. These video-coding standards often employ integer counterparts of DCT reduce computation cost and increase the speed. These integer counterparts produce approximate results often introducing mismatch between DCT and inverse DCT (IDCT) structures.

In this paper we propose the use of fixed point DCT structure in OFDM. The modifications in butterfly structure enable the use of shift and add operations which can be implemented as a pure combinational logic. The use of fixed point arithmetic logic introduces some approximation error. This approximation error makes the IDCT design non-orthogonal which is the basic requirement of ODDM system. Hence, we adjust the multiplication parameters to reduce the approximation error. The complexity has been significantly reduced to reduce the gate count and power consumption. Finally, the proposed 2D-DCT OFDM scheme is incorporated in 802.11a WLAN standard. The simulation results show improvement in bit error rate (BER) performance, while the hardware implementation shows the reduction in resource consumption. This makes the design particularly useful for application in handheld mobile devices.

In the manuscript we use the following convention to denote matrices, vectors and constants

Variables: Non capitalized, slant with normal subscripts e.g. p

Matrices: Capitalized and bold with bold subscripts e.g. $\mathbf{X}$ Vectors: Capitalized and slant with slant bold subscript "*vec*", e.g. A_{vec}

Constants: Capitalised and slant, e.g. N

2.TWO DIMENSIONAL DCT-OFDM ARCHITECTURE

2.1 Converting 1-D OFDM to 2-D OFDM

The basic idea in 2D DCT-OFDM is to break the original M point vector into a smaller $m \times n$ size matrix over which 2D forward and inverse transformation can be

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performed. In [3], it was be shown that, at transmitter end, a *M*-point vector is reshaped to matrix structure, subjected 2D IFFT, reshaped again into *M*-point vector before transmission. At the receiver end the vector is again reshaped into matrix, subjected to 2D FFT, reshaped to vector again for further analysis. In [3], it was concluded that when *M*-point vector is reshaped in to $m \times n$ size matrix, the best performance is obtained at $m = n$. Hence in effect the *M*-point vector can be reshaped into $\sqrt{M}\times\sqrt{M}$ matrix. Based on same structure, in proposed scheme, the 2D-IDCT can then be implemented as column and row wise 1D- IDCT at transmitter, while at receiver the 2D-DCT can be broken down into two processes of $\sqrt{M}$ point 1D DCT. Based on the architecture given in [3] and the above discussion the 1D-FFT OFDM is replaced by 2D-DCT OFDM in as shown in Figure 1.

From, the basic definition, $N \times N$ point 2D-DCT, **Y**, of input $N \times N$ sample, **X** is given by $\mathbf{Y} = \mathbf{AXA}^{\mathrm{T}}$, where **A** is the DCT co-efficient matrix defined as

$$\mathbf{A}_{ij} = u_i \cos\frac{(2j+1)i\pi}{2N};\text{where, } u_i = \sqrt{\frac{1}{N}}(i=0)\Big/\sqrt{\frac{2}{N}}(i>0); 0 \le i, j \le n \quad (1)$$

As evident from (1), DCT uses only real arithmetic, as opposed to the complex-valued DFT. Hence, the implementation of row and column IDCT and DCT can now be performed with significantly lesser hardware implementation cost as compared to its FFT counterpart.

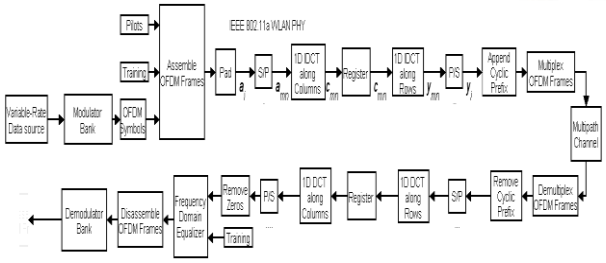

Fig. 1. Block diagram of 2D-DCT modulated OFDM

Till this point we have considered that the 1D-DCT along the row and column direction involves floating point arithmetic operations. However, for a reasonably smaller hardware implementation we need to consider the conversion of floating point implementation to integer calculation based fixed point system.

3. INTEGER BASED 1D-DCT STRUCTURE

3.1 Splitting the basic structure

From (1), the DCT coefficient matrix **A** for 8 point DCT\IDCT calculation can be given as

$$\mathbf{A} = \begin{bmatrix} F_1C_0 & F_1C_0 & F_1C_0 & F_1C_0 & F_1C_0 & F_1C_0 & F_1C_0 & F_1C_0 \\ C_1 & C_3 & C_5 & C_7 & C_9 & C_{11} & C_{13} & C_{15} \\ C_2 & C_6 & C_{10} & C_{14} & C_{18} & C_{22} & C_{26} & C_{30} \\ C_3 & C_9 & C_{15} & C_{21} & C_{27} & C_{33} & C_{39} & C_{45} \\ C_4 & C_{12} & C_{20} & C_{28} & C_{36} & C_{44} & C_{52} & C_{60} \\ C_5 & C_{15} & C_{25} & C_{35} & C_{45} & C_{55} & C_{65} & C_{75} \\ C_6 & C_{18} & C_{30} & C_{42} & C_{54} & C_{66} & C_{78} & C_{90} \\ C_7 & C_{21} & C_{35} & C_{49} & C_{63} & C_{77} & C_{91} & C_{105} \end{bmatrix} \quad (2)$$

$$F_1 = \sqrt{1/2}; \quad C_i = \frac{1}{2}\cos\left(\frac{i\pi}{16}\right)$$

Using basic matrix manipulation techniques, we can split **X** as following:

$$\mathbf{A} = \mathbf{R}_e\left(\mathbf{DFF}_1\mathbf{F}_{11} + \mathbf{DFF}_2\mathbf{F}_{22}\right)\mathbf{R}_{ee} \quad (3)$$

where,

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$$\mathbf{R}_e = \begin{bmatrix} 1&0&0&0&0&0&0&0\\ 0&0&0&0&1&0&0&0\\ 0&1&0&0&0&0&0&0\\ 0&0&0&0&0&1&0&0\\ 0&0&1&0&0&0&0&0\\ 0&0&0&0&0&0&1&0\\ 0&0&0&1&0&0&0&0\\ 0&0&0&0&0&0&0&1 \end{bmatrix}; \mathbf{R}_{ee} = \begin{bmatrix} 1&0&0&0&0&0&0&1\\ 0&1&0&0&0&0&1&0\\ 0&0&1&0&0&1&0&0\\ 0&0&0&1&1&0&0&0\\ 1&0&0&0&0&0&0&-1\\ 0&1&0&0&0&0&-1&0\\ 0&0&1&0&0&-1&0&0\\ 0&0&0&1&-1&0&0&0 \end{bmatrix}$$

$$\mathbf{DFF}_1 = \begin{bmatrix} 0&1&1&0&0&0&0&0\\ b&0&0&-b&0&0&0&0\\ 1&0&0&1&0&0&0&0\\ 0&-b&b&0&0&0&0&0\\ 0&0&0&0&0&1&d&0\\ 0&0&0&0&1&0&0&-d\\ 0&0&0&0&d&0&0&1\\ 0&0&0&0&0&-d&1&0 \end{bmatrix}; \mathbf{F}_{11} = \begin{bmatrix} a&0&0&0&0&0&0&0\\ 0&a&0&0&0&0&0&0\\ 0&0&a&0&0&0&0&0\\ 0&0&0&a&0&0&0&0\\ 0&0&0&0&c&0&0&0\\ 0&0&0&0&0&c&0&0\\ 0&0&0&0&0&0&c&0\\ 0&0&0&0&0&0&0&c \end{bmatrix};$$

$$\mathbf{DFF}_2 = \begin{bmatrix} 1&0&0&1&0&0&0&0\\ 0&e&-e&0&0&0&0&0\\ 0&-1&-1&0&0&0&0&0\\ e&0&0&-e&0&0&0&0\\ 0&0&0&0&1&0&0&g\\ 0&0&0&0&0&-g&-1&0\\ 0&0&0&0&0&-1&g&0\\ 0&0&0&0&g&0&0&-1 \end{bmatrix} \mathbf{F}_{22} = \begin{bmatrix} a&0&0&0&0&0&0&0\\ 0&a&0&0&0&0&0&0\\ 0&0&a&0&0&0&0&0\\ 0&0&0&a&0&0&0&0\\ 0&0&0&0&f&0&0&0\\ 0&0&0&0&0&f&0&0\\ 0&0&0&0&0&0&f&0\\ 0&0&0&0&0&0&0&f \end{bmatrix}$$

$a = CF_4;\ b = CF_2 / CF_4;\ c = CF_3;\ d = CF_5 / CF_3;$
$e = CF_6 / CF_4;\ f = CF_1;\ g = CF_7 / CF;$
$CF_i = \cos(i\pi/16) \qquad i = 1 \text{ to } 7$

From (3) it can be seen that splitting the DCT coefficient matrix into largely sparse matrix allows us to implement a parallel architecture. From (3) and basic 1D-DCT transform equation the IDCT – DCT pair is given as

$$\mathrm{DCT}(X_{vec}) = Y_{vec} = X_{vec}\mathbf{A}^T = X_{vec}[\mathbf{R}_{ee}{}^T(\mathbf{DFF}_1{}^T\mathbf{FF}_{11}{}^T + \mathbf{DFF}_2{}^T\mathbf{FF}_{22}{}^T)\mathbf{R}_e{}^T] \quad (4)$$

$$\mathrm{IDCT}(Y_{vec}) = X_{vec} = Y_{vec}\mathbf{A} = Y_{vec}[\mathbf{R}_e(\mathbf{DFF}_1\mathbf{FF}_{11} + \mathbf{DFF}_2\mathbf{FF}_{22})\mathbf{R}_{ee}] \quad (5)$$

Note that, $\mathbf{FF}_{11}{}^T = \mathbf{FF}_{11}$ and $\mathbf{FF}_{22}{}^T = \mathbf{FF}_{22}$

3.2 Integer 1D-DCT/IDCT structure

For the purpose of scaling and converting the floating point factors to integer factors, we define *floor* and *round* functions as follows.

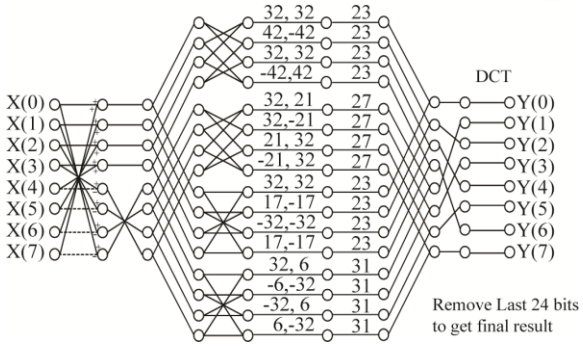

Fig. 2. Parallel architecture for 1D-DCT calculation

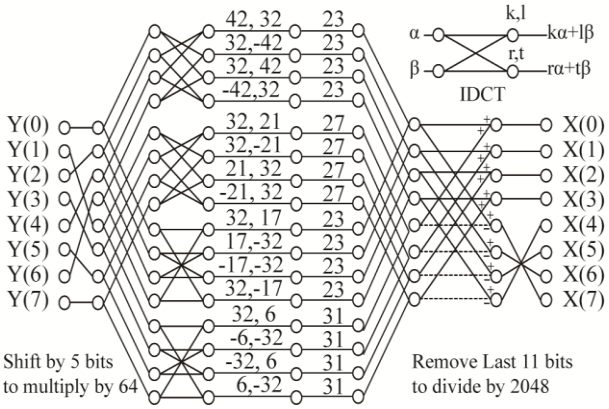

Fig. 3. Parallel architecture for 1D-IDCT calculation

floor (x) = round to the nearest lower value, e.g. 0.13, 0.15 and 0.19 all are rounded to 0.1. For binary number system let a fixed point fractional number be given as $b_i \ldots b_1 b_0 \cdot b_{-1} b_{-2} \ldots b_j$. hence, for binary number system

floor $(b_i \ldots b_1 b_0 \cdot b_{-1} b_{-2} \ldots b_j) = b_i \ldots b_1 b_0$

round (x) = round to the nearest value, e.g. 0.13 and 0.14 are rounded to 0.1, while 0.15 and 0.19 all are rounded to 0.2. For binary number system

round $(b_i \ldots b_1 b_0 \cdot b_{-1} b_{-2} \ldots b_j) = b_i \ldots b_1 b_0 + b_{-1}$

From (3), we can see that to convert the floating point numbers to integer, we need to scale and *floor* or *round* the values of a, b, c, d, e, f and g. It can be shown that if we properly choose a scaling factor S, then for

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any value v, we have $v \approx \text{round}(Sv)/S$. Here, *round* (Sv) will give us scaled integer value of v. Hence, we can convert various variables to integer as shown below

$$a = CF_4; b = round\left(CF_2 / CF_4\right); c = CF_3; d = round\left(CF_5 / CF_3\right);$$
$$e = round\left(CF_6 / CF_4\right); f = CF_1; g = round\left(CF_7 / CF_1\right);$$
$$CF_i = round\left(32 * \cos\left(i\pi/16\right)\right) \qquad i = 1 \text{ to } 7$$

Using the same analysis, we can convert the DCT\IDCT computation given in (4) and (5) to

$$DCT(X_{vec}) = Y_{vec} = X_{vec}\mathbf{A}^T = X_{vec}[\mathbf{R}_{ee}{}^T(\mathbf{SFF}_1{}^T\mathbf{SF}_{11}{}^T + \mathbf{SFF}_2{}^T\mathbf{SF}_{22}{}^T)\mathbf{R}_e{}^T]/2048 \quad (6)$$

$$IDCT(Y_{vec}) = X_{vec} = Y_{vec}\mathbf{A} = Y_{vec}[\mathbf{R}_e(\mathbf{SFF}_1\mathbf{SF}_{11} + \mathbf{SFF}_2\mathbf{SF}_{22})\mathbf{R}_{ee}]/2048 \quad (7)$$

$$\mathbf{SFF}_1 = 32*\mathbf{DFF}_1;\ \mathbf{SF}_{11} = 64*\mathbf{FF}_{11};\ \mathbf{SFF}_2 = 32*\mathbf{DFF}_2;\ \mathbf{SF}_{22} = 64*\mathbf{FF}_{22};$$

Based on (6) and (7) a parallel structure can be designed for integer based calculation of DCT\IDCT. Fig.2 and Fig.3 shows the butterfly structure to calculate 8-point DCT and IDCT respectively using integer calculations.The coefficients shown in the parallel architecture are all integer and hence a multiplication with a coefficient can be changed to shift operation. For example,

$31 \times v = (32 - 1)v = 32v - v = v_b << 5 - v_b$

where, v_b denotes the binary representation of v and $<< \mu$ denotes the right shift by μ bits. Hence all the multiplication in the 1D-DCT/IDCT computations can be changed to shift and add operations.

3.3 Integer 2D-DCT/IDCT structure

From the basic definition, $N \times N$ point 2D-DCT, **Y**, of input $N \times N$ sample, **X** is given by $\mathbf{Y} = \mathbf{AXA}^T$. For any two matrices **σ** and **δ**, $[\boldsymbol{\sigma\delta}]^T = \boldsymbol{\delta}^T\boldsymbol{\sigma}^T$, hence we have

$$\mathbf{Y} = [\mathbf{A}(\mathbf{XA})^T]^T, \quad (8)$$

where **AX** is column wise 1D-DCT of **X**. Similarly, from the basic definition, $N \times N$ point 2D-IDCT, **X**, of input $N \times N$ sample, **Y** is given by $\mathbf{Y} = \mathbf{A}^T\mathbf{XA}$,

$$\mathbf{Y} = [\mathbf{A}^T(\mathbf{A}^T\mathbf{X})^T]^T,$$

where **AX** is column wise 1D-DCT of **X**.

Hence in congruence with the earlier discussion, from (8) and (9), we can conclude that 2D-DCT/IDCT can be performed using 1D-DCT/IDCT as shown in Fig. 4.

It is important to consider the errors introduced at each 1D-DCT/IDCT stage due to approximation of scaling and converting floating point numbers to integers. It can be shown that if proper scaling factor is chosen the approximation error can be reduced to less than 2.5 percent.

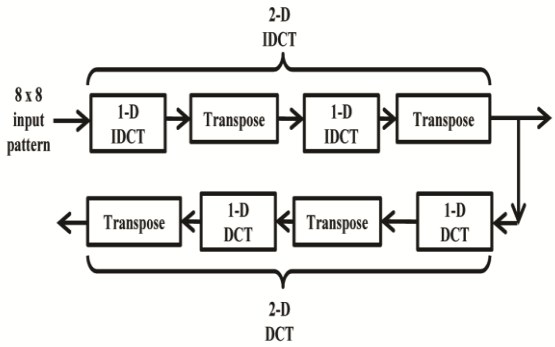

Fig. 4. Implementation of 2D-DCT/IDCT using 1D-DCT/IDCT

4. IMPLEMENTATION AND RESULT

The design presented in the previous section was used to implement a fast 8 point 1-D IDCT-DCT structure. Fig. 5 shows the MATLAB Simulink model used to verify the operation of the proposed scheme. The model presented is the physical layer of the 802.11a WLAN model. The presented model was used to find the BER performance of the proposed 2D-DCT OFDM scheme as compared to the conventional 1D-FFT OFDM system.

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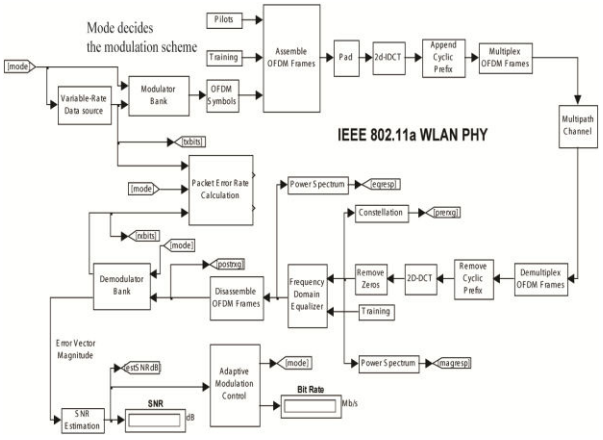

Fig. 5. 2D-DCT OFDM based IEEE 802.11a WLAN PHY SIMULINK

4.1 BER performance

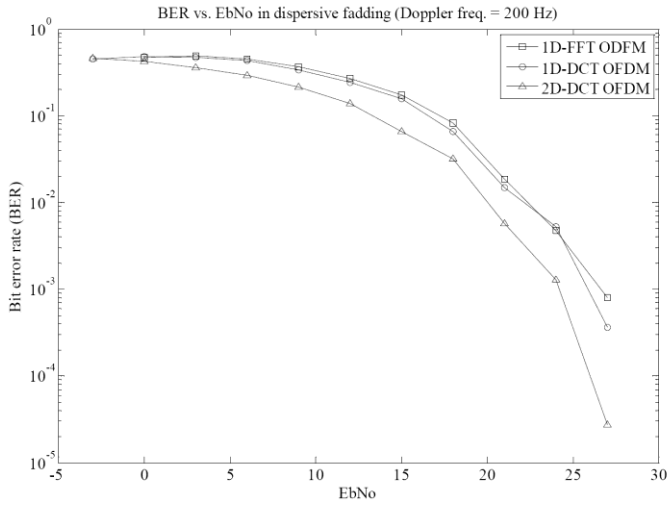

Fig. 6. Performance comparison between 2D DCT OFDM and 1D-FFT OFDM in dispersive channel (Doppler freq. = 200Hz)

BER performance comparison of the proposed 2D-DCT OFDM with 1D-DCT OFDM system and the conventional 1D-FFT OFDM system is shown in Fig. 6. It can be seen that the conversion of the floating point calculations to integer calculations have no effect on the BER performance. Similar to the results obtained in [3], the BER performance improves when the 1D-ODFM is changed to 2D-OFDM (even for the dispersive channel). Hence with the proposed implementation, better error rate performance can be achieved with reduced complexity and faster hardware implementation.

4.2 Hardware implementation

In the integer based implementations, generally used in video encoding algorithms, there is a drift between the calculated DCT/IDCT values and the theoretical values. To reduce this drift the quantizers following the DCT/IDCT block provides the necessary scaling. In the proposed scheme no such quantizer is required and it can be verified that the drift between the theoretical value and the value of DCT/IDCT obtained using proposed scheme is less than 2 percent. The presented design was used to implement integer DCT-IDCT pair. The implemented design was co-simulated using MATLAB and FPGA design board. Table I shows the gate count comparison of the proposed scheme with some of the existing schemes. The hardware comparison results indicated that due to integer based calculation the calculation speed increases.

Table 1 2D-DCT implementation Comparison

Algorithm	Equivalent gate count	Critical path (ns)	Frequency (MHz)
[9]	77,280	9.30	94.0
[10]	6212	28.30	34.8
[11]	17,035	9.67	101.50
Proposed	14,732	5.72	169.3

5. CONCLUSION

In this paper we presented the 2D-DCT based OFDM scheme. We considered the method of replacing the 1D-FFT OFDM with 2D-DCT OFDM. An integer based architecture was proposed to compute the 2D-DCT to be used in 2D-DCT OFDM.

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Integer based 2D-DCT currently used in video processing algorithm require quantizers to reduce the drift between the calculated value and the actual value. Proposed scheme does not require any quantizer and the drift from the theoretical value is less than 2 percent. The bit error performance in 802.11a WLAN model employing 2D-DCT OFDM shows that the proposed scheme can achieve better performance as compared to the conventional system. Hardware implementations show that, with the proposed scheme the resource consumption is reduced and the operating speed is increased. This comparative bit error performance with reduced resource requirement makes the proposed scheme particularly attractive for the mobile wireless applications.

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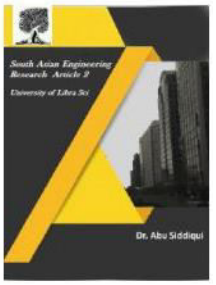

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