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ADVANCED DESIGN FOR SERIAL AND MIXED SCAN TEST USING FLIPFLOP

[1]SHAIK JAREENA, [2]B.HANISH CHAITANYA

[1]STUDENT, DEPT ECE, GVR&S COLLEGE OF ENGINEERING AND TECHNOLOGY BUDAMPADU, GUNTUR.

[2]ASSOCIATE PROFESSOR, DEPT ECE, GVR&S COLLEGE OF ENGINEERING AND TECHNOLOGY BUDAMPADU, GUNTUR.

Abstract: The simplicity of testing and high test inclusion has made it increase far reaching modern acknowledgment. Be that as it may, there are punishments related with the sequential output plan. These punishments incorporate execution debasement, test information volume, test application time, and test control scattering. The exhibition overhead of sweep configuration is because of the output multiplexers added to the contributions of each flip-flop. In the present rapid structures with least conceivable combinational profundity, the exhibition corruption brought about by the output multiplexer has turned out to be amplified. Consequently, to keep up circuit execution, the planning overhead of output configuration must be tended to. In this task, we propose another output flip-flop structure that dispenses with the presentation overhead of sequential sweep. The proposed structure expels the output multiplexer from the useful way. The proposed structure can help improve the utilitarian recurrence of execution basic plans. Moreover, the proposed structure can be utilized as a typical sweep flip-flop in the "blended output" test wherein it tends to be utilized as a sequential sweep cell just as an arbitrary access check (RAS) cell. The blended output test engineering has been executed utilizing the proposed sweep flip-flop

INTRODUCTION

With extending structure multifaceted design in present day SoC plan, various memory models with different sizes and types would be consolidated. To test most of the memory with for the most part insignificant exertion transforms into a critical issue. Worked in Self Test, or BIST, is the system of arranging additional gear and programming features into fused circuits to empower them to perform self-testing, i.e., testing of their own movement (for all intents and purposes, parametrically, or both) using their very own circuits, thusly decreasing dependence on an external motorized test equipment (ATE). BIST is a Design-for-Testability (DFT) strategy, since it makes the electrical testing of a chip less complex, faster, progressively powerful, and more affordable. The possibility of BIST is relevant to practically any kind of circuit, so its execution can vary as extensively as the thing grouped assortment that it considers.

Current VLSI circuits, e.g., data way plans, or electronic banner dealing with chips ordinarily contain number juggling modules [accumulators or calculating method of reasoning units (ALUs)]. This has ended the probability of calculating BIST (ABIST) . The basic idea of ABIST is to utilize

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2581-4575
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gatherers for worked in testing (weight of the CUT responses, or period of test structures) and has been seemed to bring about low gear overhead and low impact on the circuit common working rate.

The target of sweep configuration is to accomplish full controllability and discernibleness of each flip-flop in the plan. In a full output plan, each flip-flop is supplanted by a sweep flip-flop. A sweep flip-flop is only a muxed information ace slave based D type flip-flop. The sweep multiplexer has two sources of info: information input (D) and output input (SI). The info choice is performed utilizing a control sign called test empower (TE). In practical mode, information info is chosen and the sweep flip-flop work as an ordinary flip-flop. In test mode, check info is chosen, and all the sweep flip-flops associate in a sequential manner to frame at least one sequential move register(s). The sequential move register(s) is famously known as sweep chain(s). Every single flip-lemon of the output chain are stacked with wanted information by back to back utilization of the clock signal. A full sweep configuration decreases the consecutive test issue to combinational test issue.

The sequential output is clearly not free from downsides. There are some intrinsic punishments related with the sequential sweep. These punishments include: 1) execution overhead, 2) test information volume, 3) test control utilization, and 4) test application time. The presentation overhead of sequential output is because of the sweep multiplexer. The output multiplexer falls into each timed way and includes execution punishment of roughly two door delays. A circuit without output plan and with sweep configuration is appeared in Figure 1. As it is detectable in Figure 1a, the basic way of a successive circuit without sweep addition is chosen by the longest combinational way between two flip-flops. In any case, in a sweep embedded successive circuit (see Figure 1b) the equivalent basic way is prolonged by an output multiplexer toward the part of the arrangement way. The sweep configuration additionally includes an extra fanout at the yield of a flip-flop. Both of these variables increment the basic way delay, subsequently lessens utilitarian clock speed by 5% to 10%. This makes it important to dispose of the presentation overhead of the output multiplexer. A few arrangements have been proposed to lighten the presentation punishment of sweep structure. One such arrangement that lightens the presentation overhead, just as different punishments related with the sequential output configuration is the utilization of incomplete sweep rather than full check. In fractional output plan, just a subset of every flip-flop in Circuit-Under-Test (CUT) are supplanted by sweep flip-lemon to shape a sweep chain. This subset does exclude flip-lemon of the basic ways, subsequently lessens the presentation punishment of output. Moreover, the incomplete output plan systems likewise decrease test information volume and test application time which are straightforwardly identified with test-cost. Be that as it may, the halfway output plan methods may prompt lower issue inclusion of the CUT.

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2. FULL SCAN DESIGN

Full sweep is a DFT plot which decreases ATPG intricacy by enabling memory components to be controlled and saw during testing and test age. An entryway level structure is changed over to a full output plan by supplanting every single flip-flop (FFs) with sweep FFs, and interfacing the sweep FFs (SFFs) to make a sweep chain [1,2]. Coach Graphics DFTAdvisor device was utilized to embed sweep chains into both upgraded structures for this undertaking. In the two plans, 1,346 flip-flops were supplanted with output flip-flops.

2.1 Scan Chains

A commonplace output flip-flop is appeared in figure 1. Each embedded SFF has two additional sources of info, scan_in and scan_enable, and an extra fanout, scan_out. To shape a sweep chain, the SFFs are connected together as appeared in figure 3, and three sign are steered to I/O pins, scan_enable, scan_in, and scan_out. The output chain can be set to either ordinary or sweep mode by setting the scan_enable essential information. In ordinary mode, SFFs catch information from their information input. At the point when the circuit is set to filter mode, the sweep chain frames a move register that can be stacked and emptied sequentially utilizing scan_in and scan_out I/O pins, enabling memory components to be both controllable and discernible [1,2]. Subsequent to embeddings filter hardware into both areaOpt and delayOpt structures, two I/O pins were included, a sweep in stick and an output empower stick. The most noteworthy piece of the Memory_Address yield is utilized for sweep out in the two cases.

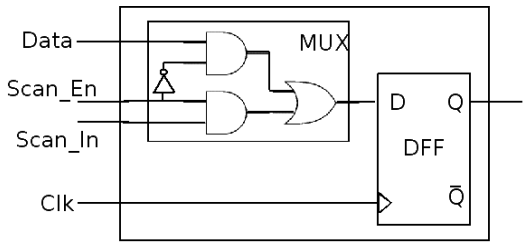

Figure 1: Typical Scan Flip-Flop

3.EXISTING SYSTEM

An ordinary output flip-flop configuration is appeared in Figure 4.1. This output cell is an ace slave hook based positive edge activated muxed input D type flip-flop . The transmission door T1 and the inverter pair associated consecutive by means of transmission entryway T2 structures the ace lock. The slave hook includes transmission door T3 and the inverter pair associated consecutive over transmission entryway T4. The multiplexer at the contribution of ace hook chooses between utilitarian information (D) and sweep input (SI) contingent on the estimation of test control sign test empower (TE). In test mode, when TE is high (1), SI is chosen and is associated with ace hook's information. At the point when the clock signal (CP) is low (0), the estimation of SI proliferates to the ace hook. In the in the mean time, the slave lock holds the incentive from past clock cycle. The worth locked into the ace spreads to slave hook when CP goes to high (1), and to the yield Q of sweep flip-flop. Correspondingly, when the test empower signal (TE) is set to 0, practical info D is chosen, and the circuit works in useful mode.

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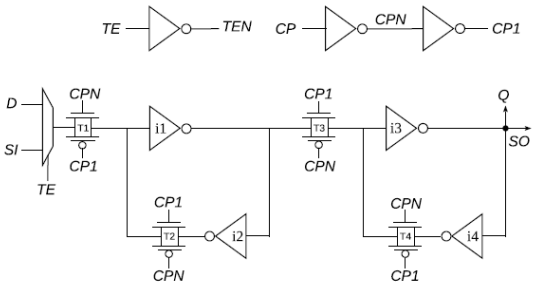

Figure 2. Conventional Scan Flip-Flop Architecture

4. PROPOSED SCAN FLIP-FLOP DESIGN

This working of the proposed sweep flip-flop in various methods of activity. The proposed sweep flip-lemon's schematic structure is appeared in Figure 3. Rather than a multiplexer at ace lock's info, the proposed structure utilizes a different way for stacking test vector esteems into the ace hook. Besides, the proposed output flip-flop utilizes an ease dynamic slave lock for moving of test vectors in the test mode. In useful mode, useful slave lock's yield Q drivesthe combinational circuit inputs. The ace lock of the proposed sweep flip-flop is shaped by transmission entryway T1, and inverter pair (i1, i2) associated consecutive by means of transmission door T2. So also, the slave lock is shaped by transmission door T3, and inverter pair (i3, i4) associated consecutive by means of transmission entryway T4. The dynamic slave hook includes transmission entryway T7 and inverter i7. The test mode way is framed by including transmission entryway T5, T6, support i5, and inverter i6 to the ace hook structure. It ought to be noticed that the additional entryways added to the ace stage to frame the test mode input way are not on the useful way. This additional hardware stays incapacitated during the useful mode, and the proposed output flip-flop goes about as a standard flip-flop. The ace hook and the slave lock are constrained by useful clock signal CP. The test mode input way is incapacitated by the test_enable cum output clock signal SCK. Note that, the SCK signal in the proposed output cell is practically equal to the test_enable sign TE, notwithstanding, rather than the regular sweep structure in which TE is an absolutely combinational sign, SCK is a low recurrence or semi consecutive signal. The SCK sign is utilized both as test control just as a low recurrence output check signal in the proposed sweep structure. Since the sweep activity is performed at a much lower recurrence, regularly at 10MHz to 50MHz, contrasted with the framework or useful clock recurrence [23], the steering of SCK as a moderate recurrence output clock sign won't present much overhead as far as territory and power. The subtleties of the working of the proposed plan in various methods of activity are clarified in the accompanying
subsections:

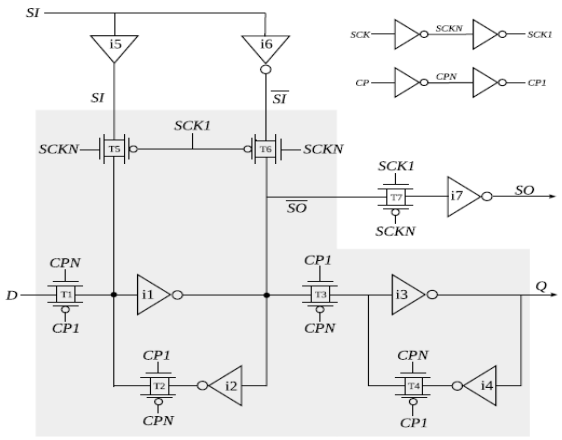

Fig. 3. Proposed scan flip-flop design.

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1) Functional Mode: The proposed output flip-flop fills in as an ordinary flip-flop in practical mode. In utilitarian mode, check clock signal SCK is kept at steady rationale high (1) level. For whatever length of time that SCK is at steady high (1) level the transmission door T5, and T6 stay incapacitated. This disengages the test mode input way from the ace structure and the proposed sweep flip-flop works as an ordinary flip-flop. The output clock signal (SCK) held at steady high (1) level shows utilitarian mode activity. During the utilitarian mode activity, the transmission door T7 consistently remains empowered. This keeps the dynamic slave hook constantly straightforward during the useful mode and makes the sweep yield (SO) flip each time at whatever point there is an adjustment in ace lock's state. Nonetheless, that isn't of any worry the extent that the utilitarian mode activity is concerned in light of the fact that the sweep yield (SO) drives just the output way which feeds the sweep input (SI) of the progressive sweep flip-flop. The sweep input way stays detached from the ace structure during the practical method of activity. The flipping of sweep yield SO will make exchanging action in the output way which additionally occurs in the traditional output structure. Since if there should arise an occurrence of traditional sweep cell the combinational burden, just as the output way, is driven by the Q yield of the output cell. In this way, in the event of ordinary sweep cell during utilitarian mode, at whatever point there will be a flipping on the Q yield, it will spread in both the combinational rationale too in the output way. Likewise, in regular output cell, the sweep multiplexer which falls in the output way would disseminate excess power in both the modes. In practical mode, the ace lock of proposed filter cell gets it's contribution from the useful information input D. At the point when clock CP is low, the estimation of practical information D proliferates into the utilitarian ace lock. At the point when CP goes to high, the worth locked into the ace engenders to useful slave hook, and to yield Q of the output cell. We confirm the said usefulness utilizing post-format recreation.

2) Test Mode: While keeping the useful clock CP held at steady high (1) level, successive use of sweep clock SCK makes the proposed output flip-failure to work in test mode. As the practical clock CP is kept high (1), the transmission door T1 consistently stays debilitated in test mode. This disengages the practical info D from the ace lock. During test mode, the ace lock gets its contribution from scan_input SI. The back to back use of sweep clock SCK loads the test esteems into the output flip-flops. As it very well may be seen in Figure 3, when SCK gets to rationale low (0), T5 and T6 get empowered, and the estimation of SI is composed into the ace lock likewise to memory compose activity.

It ought to be noticed that in test mode since CP is in every case high (1), the criticism way transmission entryway T2 consistently remains empowered. This makes the ace hook continually attempting to hold its past worth. In any case, it very well may be seen from Figure 3, the test mode input way circuit power composes the SI esteem all the

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2581-4575
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while at both info and yield hubs of inverter i1 by means of support i5 and inverter i6 separately. This makes the compose activity quicker to the extent coherent battling is concerned. At the point when the output clock SCK gets high (1), the dynamic slave hook transmission door T7 gets empowered, and the ace lock starts driving both unique slave hook inverter i7, and practical slave lock inverter i3. This proliferates the test worth hooked into the ace during the negative clock cycle, to dynamic slave lock, and to scan_output SO of the sweep cell. At the point when output clock SCK gets to rationale low (0), T7 gets handicapped, and the info parasitic capacitance of inverter i7 drives the progressive sweep cell's scan_input SI. Because of the high impedance of the inverter, the parasitic capacitance does not release promptly and takes quite a while. The parasitic capacitance release time chooses the base output clock recurrence at which sweep moving should be possible. The parasitic capacitance release time fundamentally relies on two components: all out information capacitance of inverter i7, and the charge spillage rate. Subsequently, for a specific creation process innovation with well-portrayed spillage rate, the release time can be streamlined by controlling the absolute info capacitance which thus relies on the size of inverter i7. The size of inverter i7 can be scaled according to the required least check recurrence. Be that as it may, a low move recurrence is bothersome as it expands the test time, which thus builds the test cost.

It ought to be noticed that in test mode the transmission door T3 consistently remains empowered. This keeps the practical slave hook constantly straightforward during test mode and makes the yield (Q) flip each time at whatever point there is an adjustment in ace lock's state. Each ace hook in sweep chain gets its output contribution from going before output flip-failure's SO yield, aside from the absolute first ace lock in the sweep chain which gets its test contribution from an essential info stick. The sweep yield SO of the last flip-failure of the sweep chain is associated with an essential yield stick. The moving of test vectors into the output chain is finished utilizing the dynamic slave lock. When the output chain is stacked, the test vector is propelled through the practical slave hook

5. APPLICATION OF TEST VECTORS

The proposed sweep flip-flop permits applying all sort of test vectors that can be connected utilizing a traditional output flipflop. Prior to applying any test vectors, check chain trustworthiness is confirmed by practicing sweep flush test. Sweep flush test is connected by spreading an all progress design, as 1100, through the output chain with no reaction catch cycle in the middle. The output clock SCK is constantly kept high during utilitarian mode. At the point when utilitarian clock CP is high (1), falling edge on SCK changes the circuit from practical mode to test or sweep mode. The useful clock CP is constantly kept high (1) during sweep move activity. On landing of the negative edge of SCK, the estimation of SI spreads into ace hook through test input way. Next, the rising edge on SCK moves

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2581-4575
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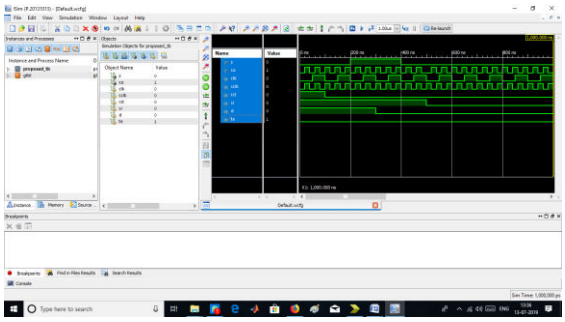
the ace hook an incentive to dynamic slave lock and to the sweep yield hub SO. By dreary utilization of sweep clock, the flush examples are spread through the output chain and saw at the essential yield stick. The perception of right info grouping at essential yield stick checks the uprightness of the sweep chain or output way.

Note that for a successive circuit component like sweep cell, the flaws are displayed at their information sources and yield terminals. In the proposed sweep cell, there are independent information sources and yields for test mode and utilitarian mode which structures the particular output way and useful way. The sweep trustworthiness test covers every single imaginable deficiency on the sweep way which contains shortcomings of test input SI, flaws of test yield SO, and issues of the output way. The sweep trustworthiness test does not cover input/yield flaws of the practical way, i.e., deficiencies of info D of the useful ace lock and blames of the yield Q of the utilitarian slave hook. As we will find in the following subsection, these deficiencies are secured during stuck to blame test application.

A. Stuck-at-Fault Test

At the point when clock CP is high (1), falling edge on sweep clock SCK demonstrates the beginning of output moving. The stuck to blame test is connected by first stacking the test vector by means of sweep moving way and after that starting the test vector through useful slave hooks. As clarified before the useful slave hook consistently stays straightforward during output moving procedure. So during the last move cum-dispatch cycle when negative edge at sweep clock SCK comes, the test vector is connected by means of yield Q of the useful slave hooks. It ought to be noticed that the test vector is propelled in last move cycle at the negative edge of the sweep clock SCK. After the dispatch of the test vector, the output clock SCK is kept high (1) to cripple the sweep input way. So as to catch the test reaction, the utilitarian clock CP is timed once. At the point when the useful clock CP gets low, the practical reaction is hooked into the ace lock through useful info D. On landing of a positive edge on the practical clock CP, the reaction is engendered to the utilitarian slave lock just as to the dynamic slave hook. When the test reaction is caught, utilitarian clock CK is kept at rationale high (1) level. This disengages the utilitarian info D from the ace lock. Presently, falling edge on sweep clock SCK changes the circuit activity from catch to move mode. At a similar negative edge on SCK, practical reaction put away in the slave lock gets moved to the useful ace hook of next output cell through the sweep input way. The emptying of test reaction is finished with the synchronous stacking of next test vector.

6. SIMULATION RESULT



7. CONCLUSION

We have proposed a sweep flip-flop plan which wipes out the presentation

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punishment of the sequential output by expelling check multiplexer from the utilitarian way. The new output flip-flop is equipped for applying every regular test and completely agrees to the customary business plan and test stream. Moreover, the proposed output flip-lemon can be utilized both as a sequential sweep cell just as a RAS cell, in the blended mode sweep test. The blended mode output configuration executed with proposed sweep flip-flop demonstrates a promising decrease in interconnect wire length, test information volume, and test application time.

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STUDENT DETAILES:

SHAIK JAREENA-172W1D6809
MAIL ID:jareeshaik123@gmail.com
BRANCH: VLSI & ES

GUIDE DETAILS:

NAME: B.HANISH CHAITANYA
MAIL ID: hanishbodepudi@gmail.com
Designation: ASSOCIATE PROFESSOR (ECE)
GVR&S COLLEGE OF ENGINEERING AND TECHNOLOGY
BUDAMPADU, GUNTUR.